

Am29F010 Data Sheet

1996 Flash Products Data Book/Handbook

INTRODUCTION

This amendment supersedes information regarding the Am29F010 device in the 1996 Flash Products Data Book/Handbook, PID 11796D. This document includes replacement pages for the Am29F010 data sheet, PID 16736F.

This amendment will be available online through the AMD World Wide Web site (<http://www.amd.com>), in addition to the literature ordering hotline. All changes

contained in this document will be included in the next release of the Flash Products Data Book/Handbook.

DOCUMENT ORGANIZATION

Table 1 lists the data book pages affected by this document and contains a description of changes for each page. In the footer of the change pages are two page numbers. The page number in parenthesis lists the corresponding page in the data book.

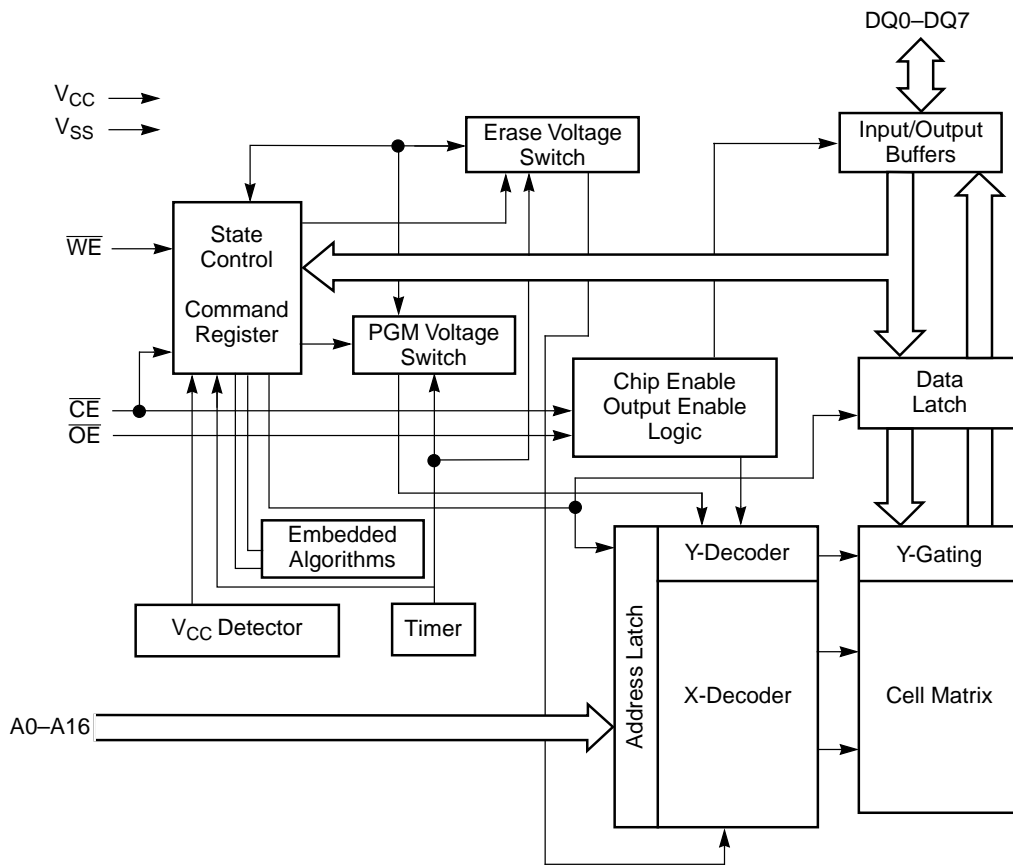
Table 1. Am29F010 Data Sheet Changes

Amendment Page	Data Book Page	Description of Changes
2	1-5	Product Selector Guide: There are now two V_{CC} supply operating ranges available for the 55 ns speed option. The PDIP package is only available in the $\pm 5\%$ V_{CC} operating range. The other packages are available in the $\pm 10\%$ operating range.
3	1-8	Ordering Information: The 45 ns speed grade is now also available in PC configuration (PDIP package, commercial temperature.)
4	1-19	Operating Ranges: V_{CC} Supply Voltages: Changed to reflect the available speed options.
5	1-23	AC Characteristics: <i>Write/Erase/Program Operations:</i> Corrected to indicate t_{VLHT} , t_{OESP} , t_{WHWH1} , and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2} .
6	1-27	AC Characteristics: <i>Write/Erase/Program Operations, Alternate \overline{CE} Controlled Writes:</i> Corrected to indicate t_{WHWH1} and t_{WHWH2} are typical values, not minimum values. Changed value for t_{WHWH2} .
7	1-29	Erase and Programming Performance: Combined chip and sector erase specifications; changed typical and maximum values. Added Note 6.

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F010				
Ordering Part No: $V_{CC} = 5.0\text{ V} \pm 5\%$	-45	-55 (P)			
		-55 (J,E,F)	-70	-90	-120
$V_{CC} = 5.0\text{ V} \pm 10\%$					
Max Access Time (ns)	45	55	70	90	120
CE (E) Access (ns)	45	55	70	90	120
OE (G) Access (ns)	25	30	30	35	50

BLOCK DIAGRAM

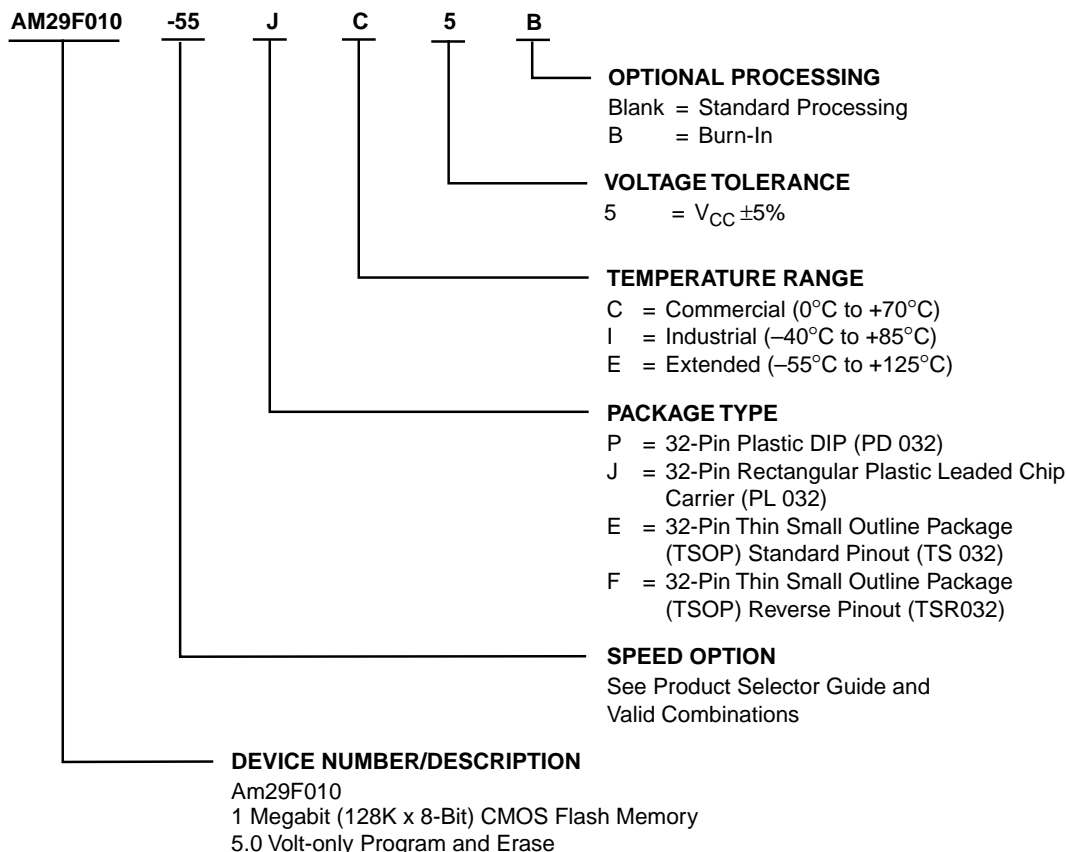


16736F-1

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F010-45 $V_{CC} = 5.0\text{ V} \pm 5\%$	PC, JC, EC, FC
AM29F010-55 $V_{CC} = 5.0\text{ V} \pm 5\%$	PC5, PC5B, PI5, PI5B
AM29F010-55 $V_{CC} = 5.0\text{ V} \pm 10\%$	JC, JCB, JI, JIB, EC, ECB, EI, EIB, FC, FCB, FI, FIB
AM29F010-70 AM29F010-90 AM29F010-120	PC, PCB, PI, PIB, PE, PEB, JC, JCB, JI, JIB, JE, JEB, EC, ECB, EI, EIB, EE, EEB, FC, FCB, FI, FIB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Plastic Packages	–65°C to +125°C
Ambient Temperature	
with Power Applied.	–55°C to +125°C
Voltage with Respect To Ground	
All pins except A9 (Note 1).	–2.0 V to +7.0 V
V _{CC} (Note 1).	–2.0 V to +7.0 V
A9 (Note 2).	–2.0 V to +14.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +12.5 V, which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A). 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for Am29F010-45, 55 (P). +4.75 V to +5.25 V

V_{CC} for Am29F010-55 (J, E, F),
70, 90, 120 –4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Description							Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)	Min	45	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	35	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	20	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	0	ns
	t_{OEHL}	Output Enable Hold Time							
		Read (Note 2)	Min	0	0	0	0	0	ns
		Toggle Bit and $\overline{\text{Data}}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{\text{OE}}$ High to $\overline{\text{WE}}$ Low)	Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Setup Time	Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time	Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	25	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	14	14	14	14	14	μs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1.3	1.3	1.3	1.3	1.3	sec
	t_{VCS}	V_{CC} Setup Time (Note 2)	Min	50	50	50	50	50	μs
	t_{VLHT}	Voltage Transition Time (Note 2)	Typ	4	4	4	4	4	μs
	t_{OESP}	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)	Typ	4	4	4	4	4	μs

Notes:

1. This does not include the preprogramming time.
2. Not 100% tested.

AC CHARACTERISTICS

Write/Erase/Program Operations

Alternate \overline{CE} Controlled Writes

Parameter Symbols		Description							Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)	Min	45	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	35	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	20	20	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (Note 2)	Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time							
		Read (Note 2)	Min	0	0	0	0	0	ns
		Toggle Bit and \overline{Data} Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHLEL}	t_{GHLEL}	Read Recover Time Before Write	Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	\overline{CE} Setup Time	Min	0	0	0	0	0	ns
t_{EHWH}	t_{WH}	\overline{CE} Hold Time	Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	25	30	35	45	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	14	14	14	14	14	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1.3	1.3	1.3	1.3	1.3	sec

Notes:

1. This does not include the preprogramming time.
2. Not 100% tested.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits		Unit	Comments
	Typ (Note 1)	Max		
Chip/Sector Erase Time	1	15 (Note 1)	sec	Excludes 00H programming prior to erasure
Byte Programming Time	14	1000 (Note 3)	μs	Excludes system-level overhead (Note 4)
Chip Programming Time	1.8	12.5 (Notes 3, 5)	sec	Excludes system-level overhead (Note 4)

Notes:

1. 25°C, 5.0 V V_{CC}, 100,000 cycles.
2. Although Embedded Algorithms allow for longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. Under worst case condition of 90°C, 4.5 V V_{CC}, 100,000 cycles.
4. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Embedded Erase algorithm, all bytes are programmed to 00H before erasure.
5. The Embedded Algorithms allow for 48 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Programming Times listed above.
6. 100,000 program/erase cycles is guaranteed; 1,000,000 program/erase cycles is typical.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V _{SS} on all pins except I/O pins (Including A9)	-1.0 V	13.5 V
Input Voltage with respect to V _{SS} on all I/O pins	-1.0 V	V _{CC} + 1.0 V
Current	-100 mA	+100 mA
Includes all pins except V _{CC} . Test conditions: V _{CC} = 5.0 V, one pin at a time.		

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	6	7.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8.5	12	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

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