High Performance PSK Demodulator in FPGA for Wireless Communication Receivers

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Phase-shift keying (PSK) demodulator is widely used in modern wireless communication receivers for waveform phase demodulation and symbol recovery. Innovative Integration (II) has developed a small footprint (<10% with Xilinx Vertex5 SX95T) PSK demodulation system that performs high speed BPSK, QPSK, and 8PSK demodulation with symbol rate up to 1.4MSPS. Together with II digital radio receiver (DRR) providing powerful channelization technique, the II-PSK-demod core can be flexibly customized as multi-channel parallel demodulation systems or as a high speed single channel broadband demodulator. With Xilinx System Generator, the design of Digital Down Converter (DDC) and the demodulation system can be rapidly prototyped and simulated in MATLAB/Simulink environment. II MATLAB/Simulink board support package (BSP) allows designers to implement a mature DSP core on X5 series board within hours, which helps to accelerate the development life cycle.

II X5 210M module is selected for PSK demodulator implementation. It features four 250 MSPS 14-bit A/D channels and a Xilinx Virtex5 SX95T FPGA. The eight lanes PCI Express interface supports continuous demodulated data stream to the host. The parallel processing capability of FPGA enables maximum channel numbers and minimum resource usage.

![II X5 210M board for PSK demodulation](image)

**Digital Channelization**

The DDC provides multi-stage channel filtering, signal compensation and shaping. It comprises a direct digital synthesizer (DDS), a cascaded integrated-comb (CIC) filter, a compensation filter (CFIR), and a programmable filter (PFIR). The DDS mixes the IF signal down to baseband, and the filters output the decimated in-band signals. CIC filter is multiplierless structures, consisting of only adders, subtracters and registers, which is a benefit for hardware implementation. CFIR is used to flatten the passband frequency response drop from CIC filter. PFIR is used to reduce the passband ripples of the CIC filter, and sharpen the transition band of the FIR filter. Using MATLAB's Filter Design and Analysis tool (FDATool) and Innovative's FrameWork Logic software, the customer can easily design and optimize each filter and visualize the final filter response.

![Digital channelization](image)
PSK Demodulation

A PSK demodulator is mainly used to restore the shifted phases that are modulated at symbol rate to the carrier signals in the transmitter, and reinterpret the phase information back to symbols. The main components included in the II-PSK-demod core are automatic gain control (AGC), matched filtering, carrier recovery, timing recovery, symbol decision and lock detection. This core can be dynamically programmable for M=2, 4, or 8 phase demodulation. Once the system is locked both demodulated In-Phase and Quadrature (I/Q) samples and hard-coded symbols are available at the outputs. Figure 3 shows the block diagram of the PSK demodulator.

The PSK demodulator processes 16 bit baseband I/Q data. The input data rate requires 8 times of symbol rate. The main data path includes a matched filter using Root Raised Cosine filter (RRC), AGC, resampler using Fractional Delay (FD) Filter and a complex multiplier. The coefficient re-loadable RRC filter is used as matched filter. Following the RRC filter the AGC is used to maximize the dynamic range of the signal magnitude and maintain an optimal output sample level for symbol decision. Outputs of the AGC is resampled by the FD filter at symbol clock, which is built by the timing recovery loop. In the timing loop error detector Maximum Likelihood based spectrum analysis technique is provided to achieve an asymptotically jitter free timing error estimate. The resampled I/Q data is multiplied by the Numerically Controlled Oscillator (NCO) outputs to remove any residual carrier frequency. Finally the symbol decision component encodes the demodulated I/Q samples into 3bit hard-coded symbols according to user input map table. The lock detector monitors the timing and carrier loop errors and asserts a lock signal when both accumulated errors are within the threshold during a predefined observation time.

![Figure 3: Block diagram of the PSK demodulation](image)

AGC, Matched Filtering and Fractional Delayed Filter

The AGC compensates any amplitude loss along the DDC and maximizes the output dynamic range. It includes a gain error detector and a loop filter that responds to the long term variation and adjusts the gain for the demodulator.

In practical communication systems, pulse shaping is used to effectively compress the transmission bandwidth. One popular pulse shaping technique is to place a root-raised-cosine (RRC) filter in the transmitter and another matched filter in the receiver to create a raised-cosine (RC) filter. The symbol values can be completely recovered without ISI if the data is sampled in the middle of the symbol period.

A fractional delayed (FD) filter with farrow structure is used in the PSK demodulation core to perform band-limited interpolation. Due to its outstanding performance of high speed online tuning and arbitrary time point interpolation, this filter, together with the timing recovery loop, allows the symbol clock to be built rapidly. Once the symbol clock in the receiver is synchronized to the transmitter, the output of this filter should be ISI free samples and can be used for carrier recovery.

Timing Recovery and Carrier Recovery Loop

The timing recovery loop is used to build a symbol clock synchronous to the one in the transmitter. The timing recovery loop includes a timing error detector (TED), a loop filter and a timing control unit. Maximum Likelihood based spectrum analysis technique is provided as the TED. It uses 4 samples per symbol to generate an asymptotically jitter free timing error estimate. This error term is processed by a second order loop filter and used as the control signals to the timing control unit. The timing control unit outputs the symbol clock and the delay control to the FD filter.
In carrier recovery component, the Costas loop is used to remove the residual carrier frequency and recover the phase information. The Costas loop includes a local NCO, a phase error detector, and a second order IIR loop filter. The detected phase error is fed back to the NCO. Once the residual frequency is locked, the mixer output is the baseband I/Q demodulated data.

Symbol Decision

The input to the symbol decision is 16 bit demodulated I/Q samples. These samples are first converted to polar coordinate representation. The phase is then rounded to 1-3 bit word based on the modulation type, which gives the binary coded symbol. An encoder logic then encodes the symbols based on the map table. The map table is a 24 bit word, which allows the user to input their own coding scheme.

Hardware Implementation

This system is simulated using Xilinx System Generator cores in MATLAB/Simulink environment. Il Board Support Package provides visual and convenient interface blocks for fast implementation. The FIFO based interface provides easy flow control along the data path. The modualized digital processing functions are built in Figure 4. Figure 5 shows an example constellation plot of the 8PSK demodulated signal.

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**Figure 4: Block diagram of the digital receiver**

**Figure 5: 8PSK constellation plot**
Performance

The BER performance of the II-PSK-demod core with AWGN is shown in Figure 6. Solid and dashed curves are theoretical BER values. Markers are II_PSK_demod core measurements. More detailed specifications are listed in Table 1.

![Figure 6: II-PSK-demod core BER performance.](image)

Table 1: II-PSK-demod core specifications.

<table>
<thead>
<tr>
<th>PSK demodulation specifications</th>
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<tbody>
<tr>
<td>Symbol Rate</td>
</tr>
<tr>
<td>Input data rate</td>
</tr>
<tr>
<td>Symbol locking range</td>
</tr>
<tr>
<td>Acquisition Time</td>
</tr>
<tr>
<td>BPSK</td>
</tr>
<tr>
<td>Level of performance</td>
</tr>
<tr>
<td>Minimum Eb/No</td>
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<tr>
<td>Carrier locking range</td>
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Conclusion

Innovative Integration has developed a high performance baseband B/Q/8PSK demodulator that works at symbol rate up to 1.4MSPS and locks within 50 msec. The PSK-demod core contains all necessary components that is required for demodulation of PSK waveforms, such as AGC, matched filtering, timing recovery, carrier recovery, symbol decision, and lock detector. The PSK-demod core can be used with II DRR multi-channel digital down converter to provide a complete solution for communication systems.