

IP-CORDIC

IP Core for Sine/Cosine Generation Using CORDIC Algorithm

FEATURES

- 16-bit, sine/cosine outputs
- Tuning Resolution $F_s/2^{24}$
- Clock rates to 450 MHz (Virtex5, -4 speed)
- 1/2 the size of Xilinx DDS core
- 0.5% of Virtex5 FPGA
- Flow control
- SFDR > 90dB
- Supports Xilinx Virtex5 FPGA
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Frequency Shifting
- FFT and spectral analysis
- Costas Loops

IMPLEMENTATION SUPPORT

- MATLAB/Simulink model
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

DESCRIPTION

The IP-CORDIC-SINE/COSINE core implements the Sine and Cosine calculation using CORDIC (COordinate Rotation Digital Computer) algorithm, which is a hardware efficient algorithm that only requires adder/subtractor, bitshift and lookup tables for computation.

The IP-CORDIC-SINE/COSINE logic core implementation is very compact, consuming less than 1% of a Virtex5 SX95T FPGA and runs at clock rates up to 450 MHz (-4 speed grade). The spectral purity exceeds 85dB (SFDR) for the 16-bit version. This is achieved using propriety algorithms that are optimized for efficient use of the FPGA resources and capabilities. Another advantage of the IP-CORDIC-SINE/COSINE core is that the data flow can be enabled to match data rates for non-continuous data flow, common in multiple channel systems.

The core is targeted at the Xilinx Virtex5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

The IP-CORDIC core can be customized for higher SFDR and resolution or ported to other devices. Contact sales for application support.

Simulation models for system design are provided as fixed point or floating point C and MATLAB. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.



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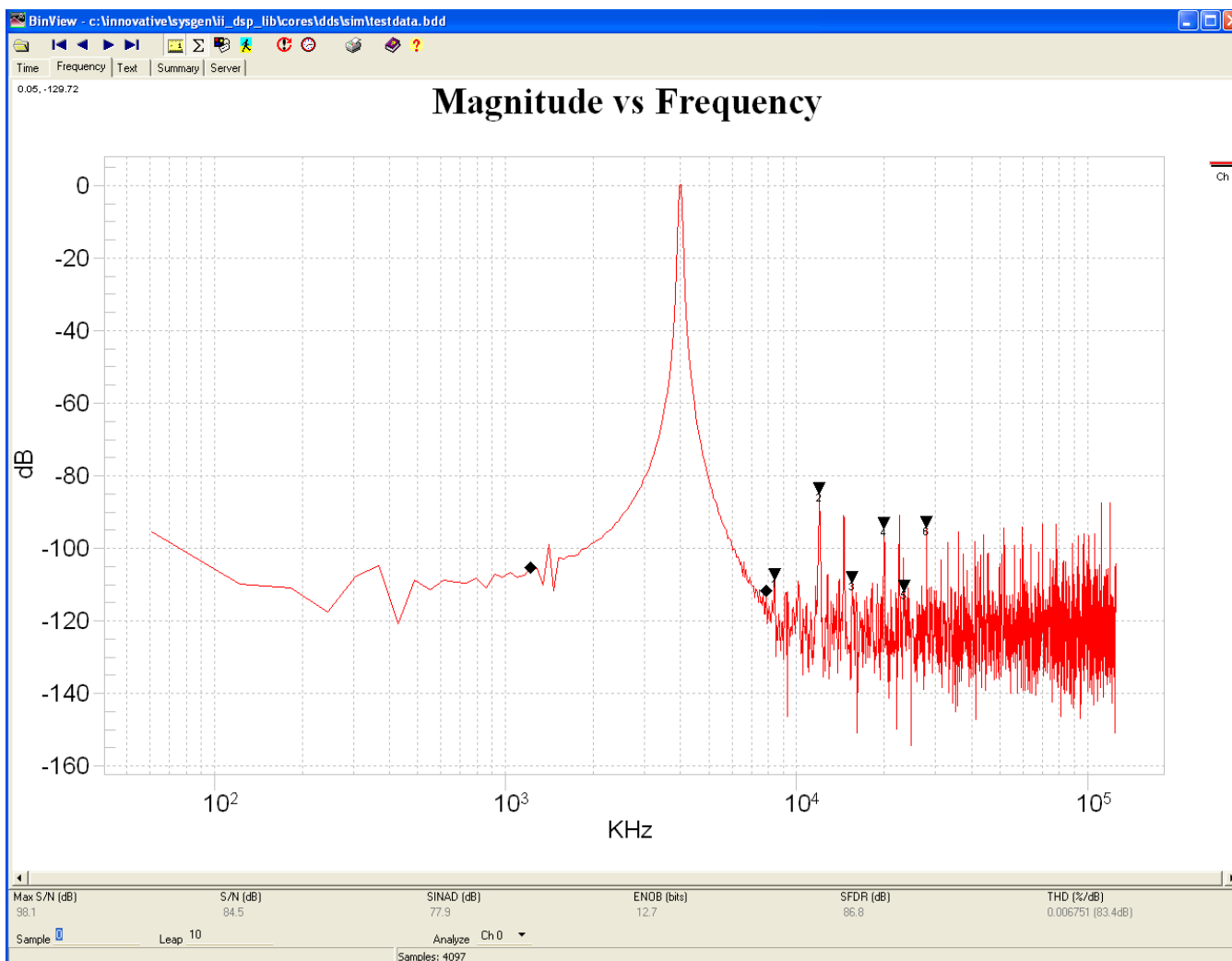
IP-CORDIC

ORDERING INFORMATION

Product	Part Number	Description
IP-Windowing	58013	IP-CORIDC, IP core for sine and cosine generation using CORDIC algorithm. Netlist version.

Performance

Frequency spectrum of a 4MHz sinusoidal signal.



IP-CORDIC

Standard Features

Inputs	
Inputs	Phase
Input Format	24-bit, 2's complement
Outputs	
Outputs	Sine/Cosine
Output Format	16-bit, 2's complement
Output Rate	$F_s/2$ (225 MHz max, Virtex5 -4 speed grade)
Tuning Resolution	$F_s/(2^{24})$
Output Latency	10 clocks

Device Utilization

Element	FPGA Resource	Virtex5 SX95T
LUT	261	0.44%
FF	251	0.42%
DSP48E	0	0%
BlockRAM	1	0.41%

Port Description

Signal	Size	IO	Description
RESET	1	I	Synchronous reset, active high.
CLK	1	I	clock.
DATA	24	I	Phase input
DATA_WE	1	I	Phase write strobe
SIN	16	O	Sine output
COS	16	O	Cosine output
VALID	1	O	Data valid

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