IP-DDC-2GSPS

v1.2

2 GSPS Digital Down Conversion Core for FPGA with Frequency Agile Bandpass Filter

FEATURES

- Four individually tuned DDC channels
- One 16 bit input @ Max 2 GSPS
- Tuning resolution up to 0.4657 Hz
- SFDR 96 dB for 16 bits input
- Decimation range from 128 to 32768
- Programmable 48 tap frequency agile bandpass filter (16 bit)
- Programmable 20 tap FIR (18 bit)
- Programmable 80 tap FIR (18 bit)
- Clock/sync bus for multi-modules synchronization
- DDC gain control up to 60 dB gain
- DDC Overflow indicator
- DC remover
- Embedded power meter (-77dBm ~ 13dBm)
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Frequency Agile Radio
- Direct RF Sampling Receiver
- Image Processing
- Spectrum Analysis

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes

Description

The IP-DDC-2GSPS core has four DC-RF frequency agile digital down conversion channels. The core can process up to 2 GSPS input data. As a flexible front-end to receivers and imaging devices, this core implements the frequency translation for baseband signal recovery as FPGA firmware.

The DDC is composed of a front-end tuning stage and a multiplexed DDC. The front-end tuning stage implements a frequency agile complex bandpass filter which is runtime tuned from DC to Fs/2 with Fs/2^32 tuning resolution, where Fs is the A/D sampling frequency. The bandpass filter uses parallel processing structures so that the input rate can be up to 2 GSPS. At the output of the filter the data rate is reduced to Fs/8. The passband signal is then sent to the four channel DDC for channelization and further decimation. In the DDC stage each channel has its own tuning frequency, filtering, and gain control. The channel rejection is up to 80dB, and the SFDR is over 96 dB for the 16 bit inputs. Gain adjustment is allowed after each decimation filter, and an overflow indicator is provided at each point to prevent arithmetic overflow. A power meter is attached to the front-end ADC raw data or the DDC output data, which allows the user to monitor both the wideband input power and the narrowband output power. A DC remover is placed at the end of the data path to remove any DC offsets present in the ADC input and in the computation process of the DDC due to truncation and asymmetric rounding.

A Matlab configuration file is provided along with the IP core to help the user easily design the decimation filters, visualize the filter response, and create filter configuration files.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and consumes about 31% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

04/01/11

IP-DDC-2GSPS

Ordering Information

Product	Part Number	Description
IP-DDC-2GSPS	58016-0	Netlist version bundled with X6/X5 boards
	58016-1	Netlist Version Only
	58016-2	Source Code Version

Table 1. Product information

Block Diagram

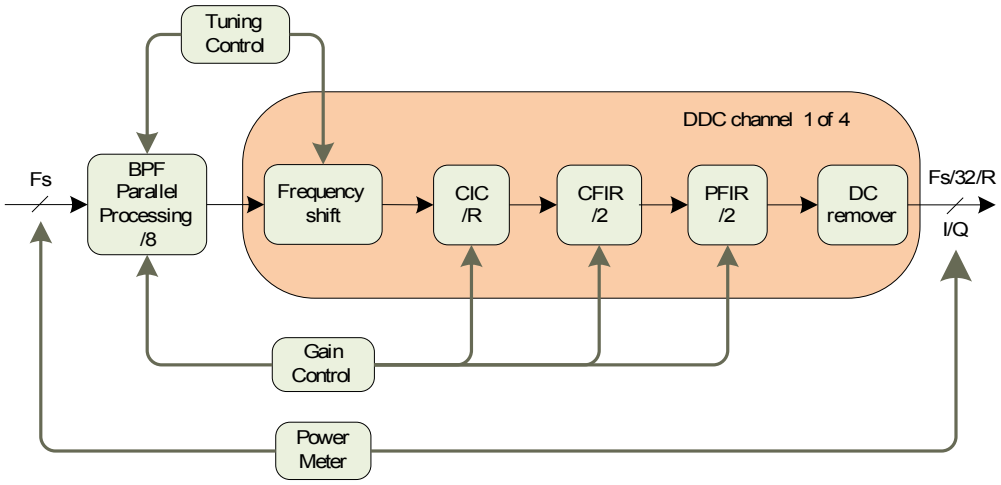

Figure 1. IP-DDC-2GSPS block diagram

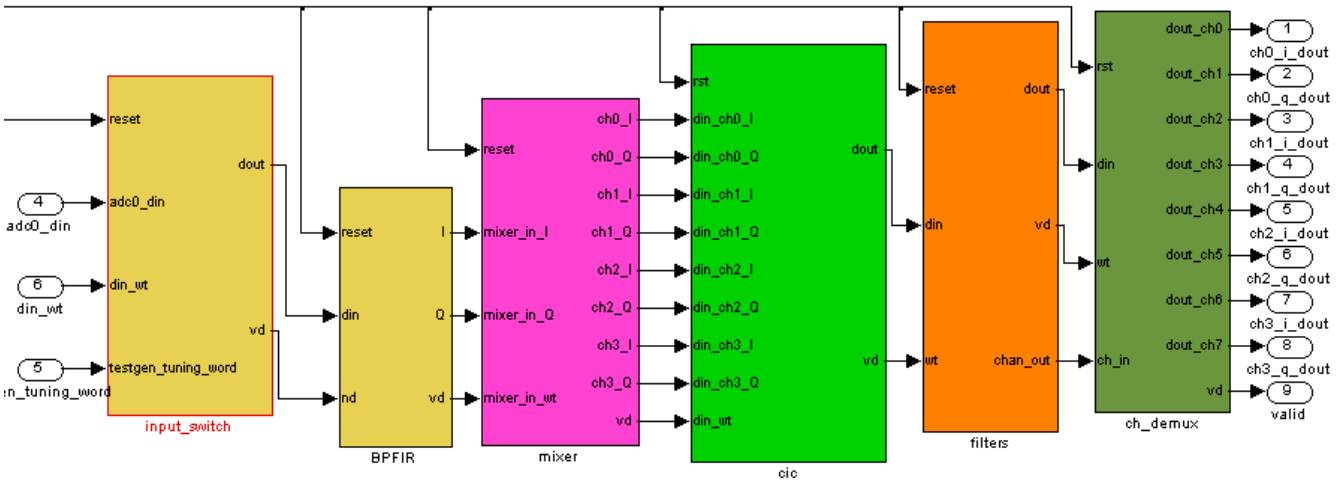

Figure 2. MATLAB/Simulink project of IP-DDC-2GSPS

IP-DDC-2GSPS

Port Description

Signal	Size	IO	Description
SYST_CLK	1	I	System clock for the design. All the design operates on rising edge of SYST_CLK.
RESET	1	I	IP synchronous reset. Reset active level is high (SCLR=1).
DDC_SYNC_IN	1	I	DDC channel synchronization. Active level high.
ADC_DIN	16	I	Real input of the IP (k ranging from 0 to 3). Signed 16 bits 2's complement format. Sampled by the IP when ADC_K_WT=1.
ADC_WT	1	I	Valid signal for input ADC_DIN. Active level high.
CTUNING_WORD	32	I	Programming bus for the Frequency Shift unit of the bandpass filter. Computed and formatted by the IP Driver.
CTUNING_WORD_WT	1	I	Valid signal for CTUNING_WORD. Active level high.
TUNING_WORD	32	I	Programming bus for the Frequency Shift unit of channel i. Computed and formatted by the IP Driver.
CHANNEL_NUM	7	I	Channel number. Used to specify the channel number for each above programmable bus.
TUNING_WORD_WT	1	I	Valid signal for TUNING_WORD. Active level high.
CIC_RATE	10	I	Programming bus for the CIC decimation rate.
CIC_RATE_WT	1	I	Valid signal for CIC_RATE. Active level high.
BPFIR_BSTART	8	I	Programming bus for BPFIR gain control. Computed and formatted by the IP Driver.
CIC_BSTART	8	I	Programming bus for CIC gain control. Computed and formatted by the IP Driver.
CFIR_BSTART	8	I	Programming bus for CFIR gain control. Computed and formatted by the IP Driver.
PFIR_BSTART	8	I	Programming bus for PFIR gain control. Computed and formatted by the IP Driver.
BPFIR_COEF_DATA	16	I	Programming bus for the BPFIR coefficient load. Computed and formatted by the IP Driver.
BPFIR_COEF_WT	1	I	Valid signal for BPFIR_COEF_DATA. Active level high.
CFIR_COEF_DATA	18	I	Programming bus for the CFIR coefficient load. Computed and formatted by the IP Driver.
CFIR_COEF_WT	1	I	Valid signal for CFIR_COEF_DATA. Active level high.
PFIR_COEF_DATA	18	I	Programming bus for the PFIR coefficient load. Computed and formatted by the IP Driver.
PFIR_COEF_WT	1	I	Valid signal for PFIR_COEF_DATA. Active level high.
PMETER_ACC_PTS	5	I	Integration points for the power meter accumulator.
PMETER_SRC_SEL	12	I	Power meter source select.
DC_REMOVAL	1	I	Bypass DC remover, 1-bypass.
OVFLO_RD	1	I	Overflow indicator read. Active level high.
DOUT_I_k	16	O	Channel k data output. Signed 16 bits 2's complement format.
DOUT_Q_k	16	O	Channel k data output. Signed 16 bits 2's complement format.
VD	1	O	Valid signal for output DOUT_I and DOUT_Q. VD is active high.
OVFLO	3	O	Overflow indicator for each decimation filter. Active level high.
PMETER_DOUT	16	O	Power meter output.

Table 2. I/O port table

Example Implementation

The front-end complex bandpass filter is runtime tunable from -Fs/2 to Fs/2. The filter response is shown in Figure 3. The input rate Fs is 2 GHz, and the tuning frequency sweeps from DC to 800MHz. The bandwidth is 120 MHz.

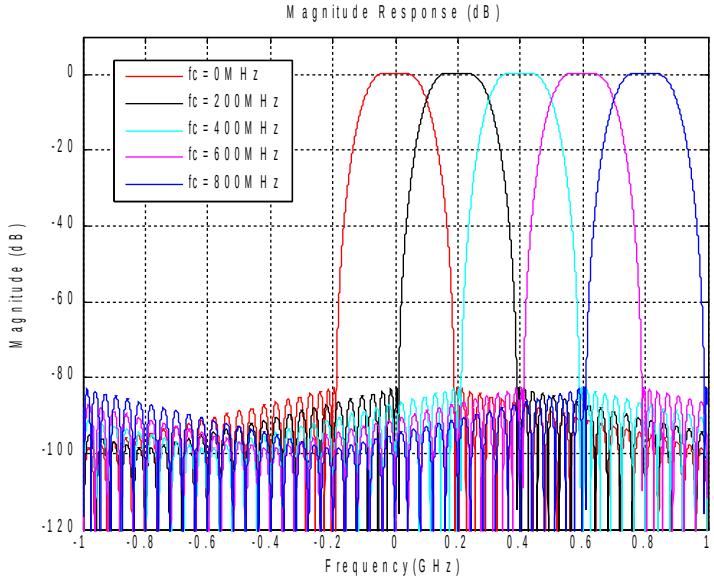

Figure 3. Bandpass filter output response

The DDC performs frequency translation and data rate reduction. Figure 4 shows the overall DDC channel response.

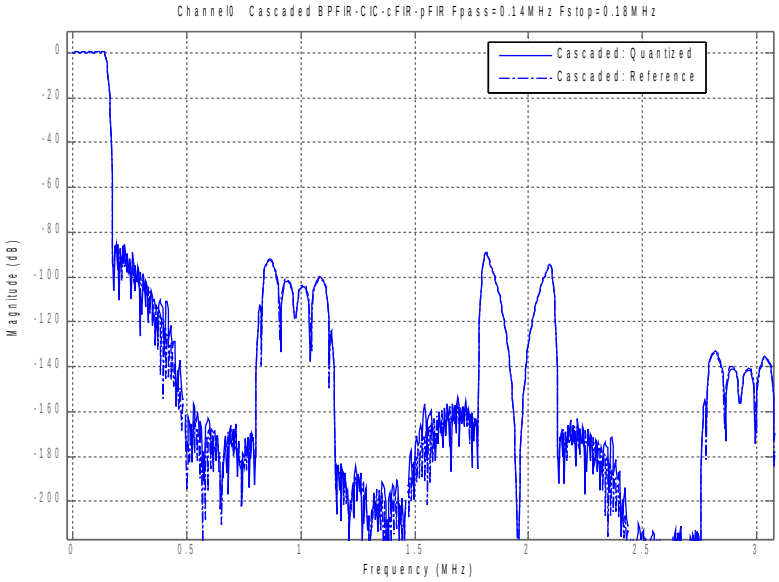

Figure 4. Overall DDC filter response

IP-DDC-2GSPS

Standard Features

Inputs	
Input Ch. Num.	1
Input Format	16-bit, 2's complement, real
Input Rate	2 GHz maximum @ 250 MHz clock*
Outputs	
Output Ch. Num.	4
Output Format	16-bit, 2's complement, I/Q
Output Rate	Fs/128 to Fs/32768
Channel Tuning	
Tuning Range	DC to Fs/2
Tuning Resolution	Fs/2^32
Front-end Bandpass Filter	
Taps	48; programmable
Taps Resolution	16 bit
Compensation Filter	
Taps	20; programmable
Taps Resolution	18 bit
Programmable Filter	
Taps	80; programmable
Taps Resolution	18 bit
Other	
Gain Range	0 to 60 dB
Overflow Indicator	Available after each filter
Power Meter	Available for DDC inputs/outputs

*Note: Higher input sample rate can be achieved by increasing the clock of the core.

Performance	
SFDR	> 96 dB (16 bit input)
S/N	Up to 80 dB

Device Utilization		
Element	FPGA Resource	Virtex-5 SX95T
FF	18.6K	31%
LUT	13.6K	23%
DSP48E	157	24%
BlockRAM	34	13%

IP-DDC-2GSPS

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