

IP-DDC4i



v1.2

Four Independent Channels Digital Down Conversion Core for FPGA

FEATURES

- Four independent channels, 24 bit DDC
- Four 16 bit inputs @ Max 250 MSPS
- Tuning resolution up to 0.0582 Hz
- SFDR >115 dB for 16 bits input
- Independent decimation range from 16 to 32768
- Programmable 20 tap CFIR (18 bit)
- Programmable 80 tap PFIR (18 bit)
- Clock/sync bus for multi-modules synchronization
- DDC gain control up to 60 dB gain
- DDC Overflow indicator
- DC remover
- Embedded power meter (-77dBm ~ 13dBm)
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Digital Receivers
- Image Processing
- Spectrum Analysis

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes



Description

The IP-DDC4i core has four independent output channels of digital down conversion (DDC). As a flexible front-end to receivers and imaging devices, this core implements the frequency translation for baseband signal recovery as FPGA firmware.

Each of the four DDCs has its own programmable tuning frequency, filtering, gain control, and decimation setting, supporting four independent output bandwidths. Each DDC channel tunes to a band through a programmable 32-bit tuner that ranges from DC to $F_s/2$, where F_s is the A/D sampling frequency. The decimation filters are composed of a CIC compiler, a compensation filter (CFIR) and a programmable filter (PFIR). The CIC compiler is programmable to provide a decimation rate from 4 to 8192, while the CFIR and PFIR are both decimation by 2 filters. This gives a total decimation of 16 to 32768 for each channel. The channel rejection is up to 90dB, and the SFDR is over 115 dB for the 16 bit inputs. Gain adjustment is allowed after each decimation filter, and an overflow indicator is provided to prevent arithmetic overflow. A power meter is attached to the DDC input and output data, which allows the user to monitor both the wideband input power and the narrowband output power.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and consumes about 41% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

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04/07/11

IP-DDC4i

Ordering Information

Product	Part Number	Description
IP-DDC4i	58014-0	Netlist version bundled with X6/X5 boards
	58014-1	Netlist Version Only
	58014-2	Source Code Version

Table 1. Product information

Block Diagram

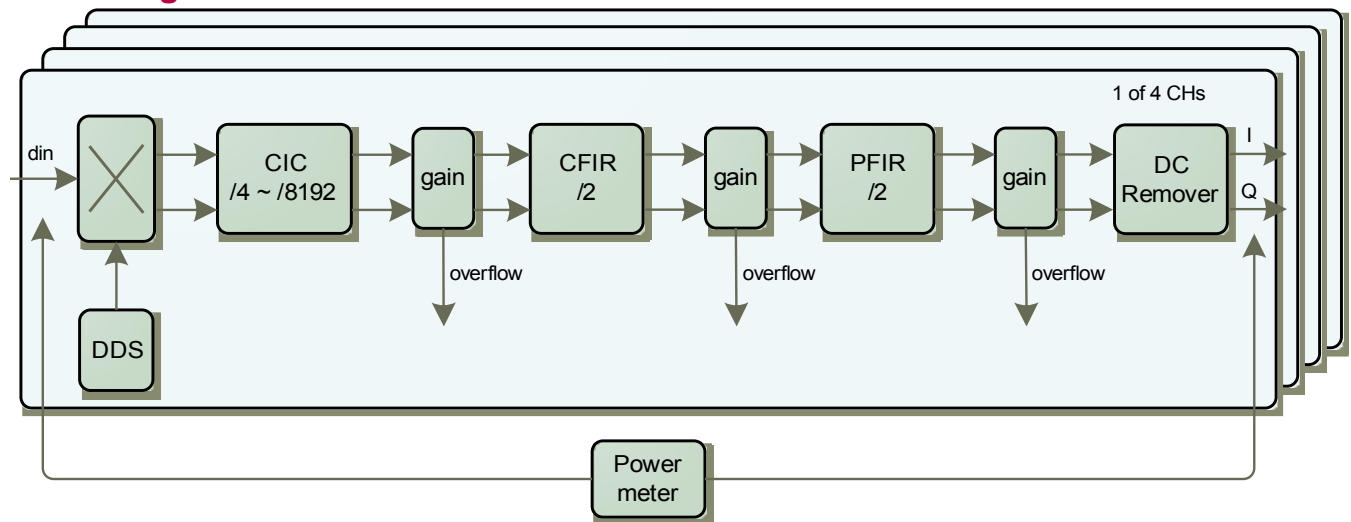


Figure 1. IP-DDC4i block diagram

IP-DDC4i

Port Description

Signal	Size	IO	Description
SYST_CLK	1	I	System clock for the design. All the design operates on rising edge of SYST_CLK.
SCLR	1	I	IP synchronous reset. Reset active level is high (SCLR=1).
ADC_K_DIN	16	I	Real input k of the IP (k ranging from 0 to 3). Signed 16 bits 2's complement format. Sampled by the IP when ADC_K_WT=1.
ADC_K_WT	1	I	Valid signal for input ADC_K_DIN. Active level high.
ADC_SEL	3	I	Programming bus for input source selection. ADC_SEL=0~3 selects from ADC0 to ADC3 inputs, ADC_SEL=4 selects the test sine wave as input.
ADC_SEL_WT	1	I	Valid signal for ADC_SEL. Active level high.
TUNING_WORD	32	I	Programming bus for the Frequency Shift unit of channel i. Computed and formatted by the IP Driver.
TUNING_WORD_WT	1	I	Valid signal for TUNING_WORD. Active level high.
CIC_R	14	I	Programming bus for CIC rate. Computed and formatted by the IP Driver.
CIC_GAIN	7	I	Programming bus for CIC gain control. Computed and formatted by the IP Driver.
CIC_R_WT	1	I	Valid signal for CIC_R and CIC_GAIN. Active level high.
CFIR_GAIN	7	I	Programming bus for CFIR gain control. Computed and formatted by the IP Driver.
PFIR_GAIN	7	I	Programming bus for PFIR gain control. Computed and formatted by the IP Driver.
FIR_GAIN_WT	1	I	Valid signal for CFIR_GAIN and PFIR_GAIN. Active level high.
CHANNEL_NUM	2	I	Channel number. Used to specify the channel number for each above programmable bus.
CFIR_COEF_DATA	16	I	Programming bus for the CFIR coefficient load. Computed and formatted by the IP Driver.
CFIR_COEF_WT	1	I	Valid signal for CFIR_COEF_DATA. Active level high.
PFIR_COEF_DATA	16	I	Programming bus for the PFIR coefficient load. Computed and formatted by the IP Driver.
PFIR_COEF_WT	1	I	Valid signal for PFIR_COEF_DATA. Active level high.
TESTGEN_TUNING_WORD	32	I	Tuning frequency for the test sine wave generator
SYNC	1	I	Clock/sync for multi-channel synchronization. Active level high.
CH_K_DOUT	16	O	Complex output k of the IP (k ranging from 0 to 3). Signed 16 bits 2's complement format.
CH_K_VALID	4	O	Valid signal for output CH_K_DOUT. VALID(k) is the valid signal for CH_K_DOUT. VALID(k) is active high.
OVFLO_K	3	O	Overflow indicator for each decimation filter. Active level high.
POWER_METER_K	16	O	Power meter output.

Table 2. I/O port table

IP-DDC4i

Example Implementation

This example shows the GSM receiver implementation of IP-DDC4i on Innovative X5-210M board.

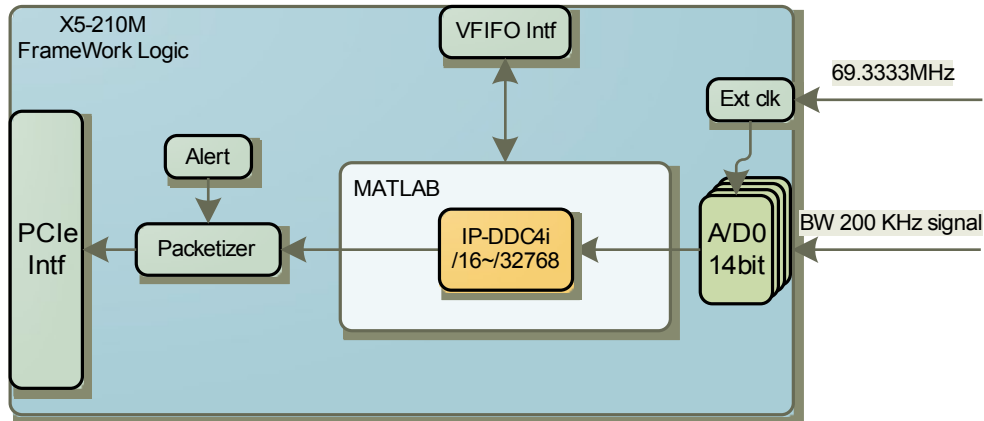


Figure 2. GSM DDC receiver using IP-DDC4i on X5-210M

Parameter	Value
Channel Bandwidth	200 KHz
Baseband Symbol Rate	270.8333 KSPS
IF Sample Rate	69.3333 MSPS
SFDR	Up to 115 dB

Table 3. GSM receiver specification

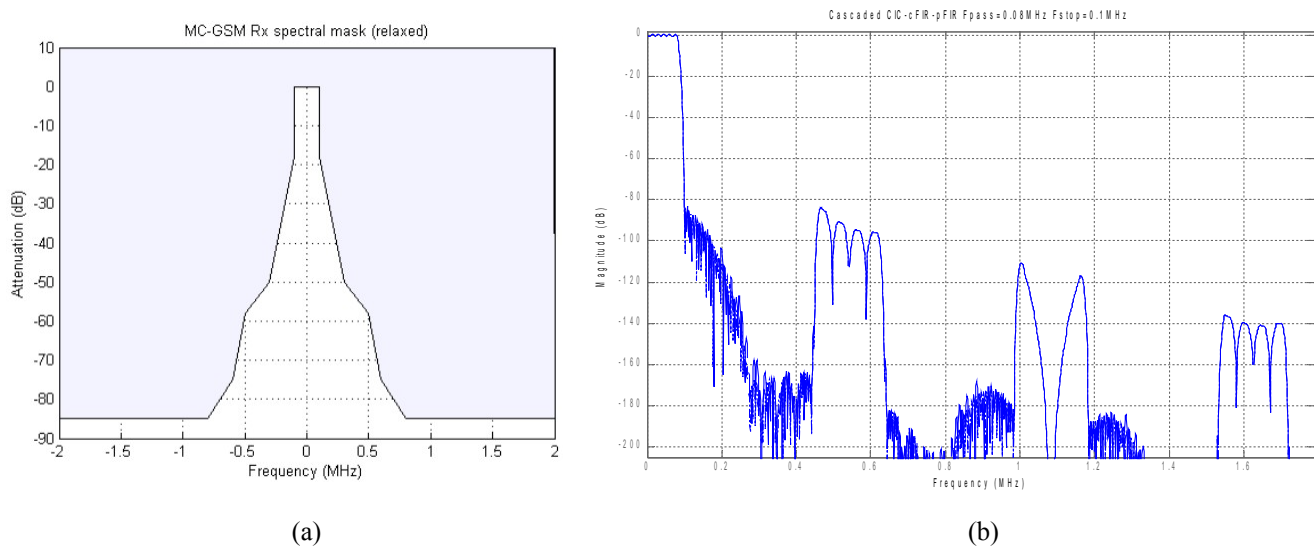


Figure 3. (a) Desired GSM spectral mask, see [Ref 1]; (b) designed DDC frequency response.

IP-DDC4i

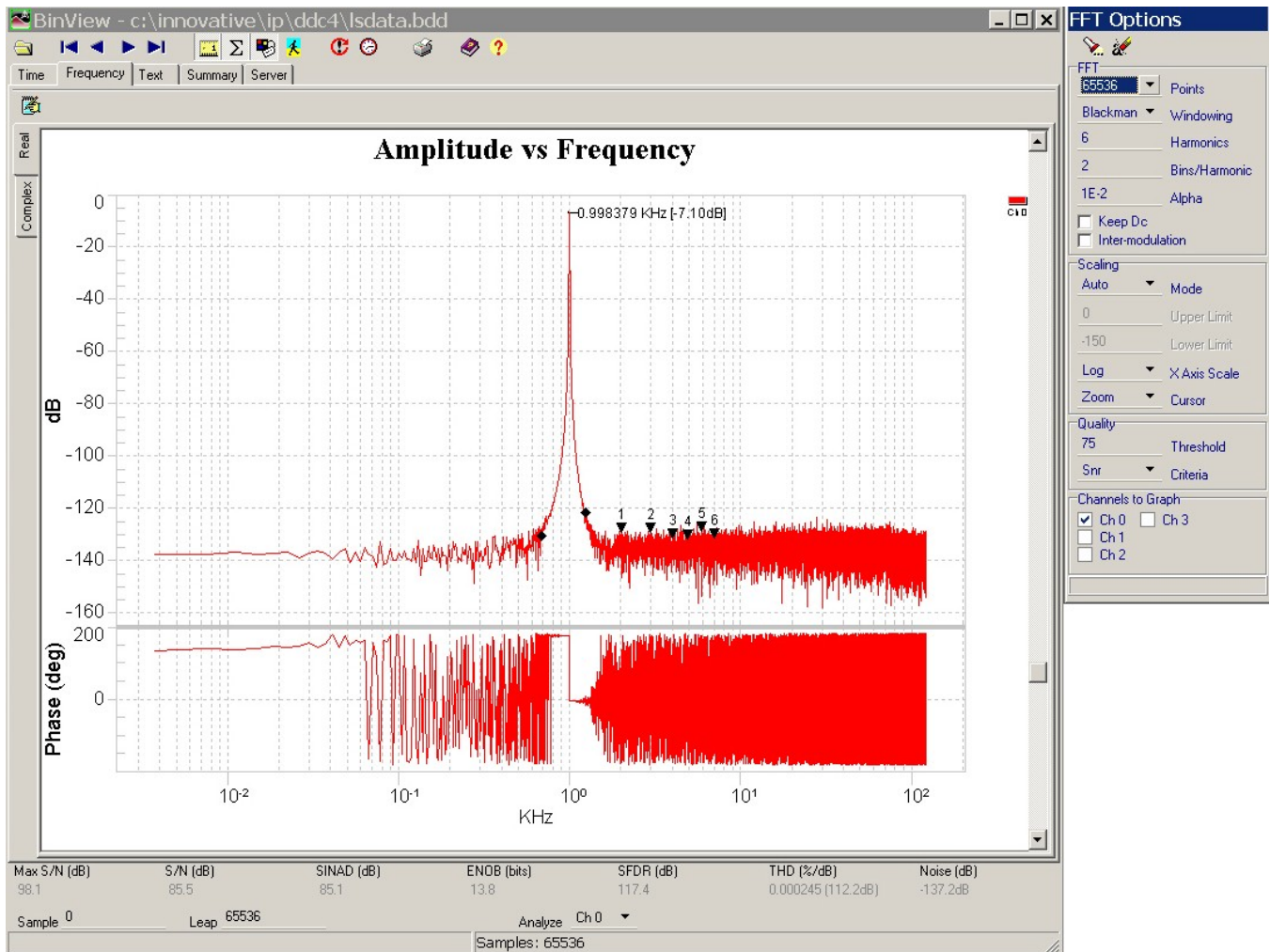


Figure 4. Typical core performance

IP-DDC4i

Standard Features

Inputs	
Input Ch. Num.	4
Input Format	16-bit, 2's complement, real
Input Rate	250 MHz maximum @ 250 MHz clock *
Outputs	
Output Ch. Num.	4
Output Format	24-bit, 2's complement, I/Q
Output Rate	Fs/16 to Fs/32768
Channel Tuning	
Tuning Range	DC to Fs/2
Tuning Resolution	Fs/2 ³²
CIC Filter	
Stage	4
Differential Delay	2
Decimation Rate	4 to 8192; programmable
Compensation Filter	
Taps	20; programmable
Taps Resolution	18 bit
Programmable Filter	
Taps	80; programmable
Taps Resolution	18 bit
Other	
Spectral Inversion	Available
Gain Range	0 to 60 dB
Overflow Indicator	Available after each filter
Power Meter	Available for DDC inputs/outputs

* Note: Higher input sample rate can be achieved by increasing the clock of the core.

Performance	
SFDR	> 115 dB (16 bit input)
S/N	Up to 90 dB

Device Utilization		
Element	FPGA Resource	Virtex-5 SX95T
FF	17561	29%
LUT	11767	19%
DSP48E	180	28%
BlockRAM	58	23%
Element	FPGA Resource	Virtex-6 LX240T
FF	13629	4%
LUT	9337	6%
DSP48E	180	23%
BlockRAM	70	16%

Reference

1. Creaney S. & Kostarnov, I. (2008). *Designing Efficient Digital Up and Down Converters for Narrowband Systems*. Retrieved from Xilinx, Inc. Xilinx, Inc website: http://www.xilinx.com/support/documentation/application_notes/xapp1113.pdf

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