

IP-TINY-DDS



v1.0

Small Footprint DDS with >90 dB SFDR at update rates to 450 MHz

FEATURES

- Waveform generator implemented as Direct Digital Synthesizer core
- 16-bit, sine/cosine outputs
- Tuning Resolution $F_s/2^{32}$
- Clock rates to 450 MHz (Virtex5, -4 speed)
- 1/2 the size of Xilinx DDS core
- Flow control
- SFDR > 90dB
- Supports Xilinx Virtex5 FPGA
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Wireless receivers
- Frequency translation
- Waveform Generation

IMPLEMENTATION SUPPORT

- MATLAB
- Testbench with test vectors
- Implementation control files
- User and implementation guide
- Application engineering support hotline/email

DESCRIPTION

The IP-TINY-DDS core is a programmable Direct Digital Synthesizer (DDS) that generates sine and cosine outputs with a spectral purity above 90 dB.

The IP-DDS logic core logic implementation is 1/3 the size and runs at 2x higher clock rates than the Xilinx core, while providing equivalent spectral purity and resolution. This is achieved using propriety algorithms that are optimized for efficient use of the FPGA resources and capabilities. Another advantage of the IP- DDS core is that the data flow can be enabled to match data rates for non-continuous data flow, common in multiple channel systems.

The core is targeted at the Xilinx Virtex5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point or floating point C and MATLAB. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.



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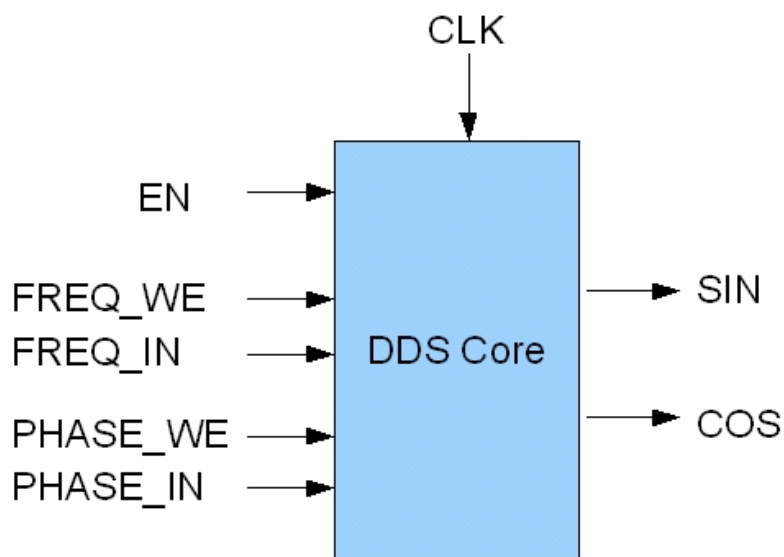
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IP-TINY-DDS

ORDERING INFORMATION

Product	Part Number	Description
IP-TINY DDS	58003	IP core for DDS function, netlist version, Virtex SX95T target

Block diagram



Port Descriptions

Signal	Size	IO	Description
RESET	1	I	Asynchronous reset, active high.
CLK	1	I	clock.
EN	1	I	Enable DDS to run, active high.
FREQ_WE	1	I	Frequency write enable
FREQ_IN	32	I	Frequency input
PHASE_WE	1	I	Phase write enable
PHASE_IN	32	I	Phase offset control.
SIN	16	O	Sine output
COS	16	O	Cosine output

IP-TINY-DDS

Standard Features

Inputs	
Data Inputs	Phase and Frequency adjust
Input Format	32-bit
Clock Rate (Fs)	450 MHz maximum (-4 device speed grade)
Outputs	
Outputs	sin and cosine
Output Format	16-bit, 2's complement
Output Rate	Fs/2 (225 MHz max, Virtex5 -4 speed grade)
Tuning Resolution	Fs/2 ³²
Output latency	6*Fs

Performance	
SFDR	>=90 dB

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
LUT	92	0.16%
FF	300	0.51%
DSP48E	0	0%
BlockRAM	1	0.41%

IP-TINY-DDS

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