IP-DUC

v1.0

Single Channel Digital Up Conversion Core for FPGA

FEATURES

- Single channel DUC
- 16 bit @ Max 250 MSPS Output Rate
- SFDR >115 dB for 16 bits output
- Tuning resolution up to 0.0582 Hz
- Interpolation range from 2 to 32768
- Programmable 20 tap CFIR (18 bit)
- Programmable 80 tap PFIR (18 bit)
- Embedded spectrum inversion
- Bypass interpolation filters capability
- Gain control up to 60 dB gain
- Overflow indicator
- Embedded power meter (-77dBm ~ 13dBm)
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Digital Transmitter
- Radar Applications
- High Speed Data Playback
- Wireless IP Development

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes

Description

The IP-DUC core has the single output channel of digital up-conversion (DUC). As a flexible front-end of transmitter, this core implements the frequency translation for baseband signal recovery as the FPGA firmware.

The DUC has programmable tuning frequency, filtering, gain control, and interpolation settings, supporting output bandwidth up to 125 MHz when the output data rate is 250 MSPS. The interpolation filters are composed of a CIC filter, a compensation filter (CFIR), and a programmable filter (PFIR). The CIC filter is programmable to provide the interpolation rate from 4 to 8192, while the CFIR and PFIR are both interpolation by 2 filters. This gives a total interpolation of 2 to 32768 for the channel with the bypass capability of each filter. The filter output is modulated to the IF through a programmable 32-bit tuner that ranges from DC to Fs/2, where Fs is the DUC output rate to the DAC. Gain adjustment is allowed after each interpolation filter, and an overflow indicator is provided to prevent arithmetic overflow. A power meter is attached to the DUC input and output data, which allows the user to monitor both the wideband output power and the narrowband input power.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and consumes about 12% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex-5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

06/01/11

IP-DUC

Ordering Information

Product	Part Number	Description
IP-DUC	58036-0	Netlist version bundled with X6/X5 boards
	58036-1	Netlist Version Only
	58036-2	Source Code Version

Table 1. Product information

IP-DUC

Block Diagram

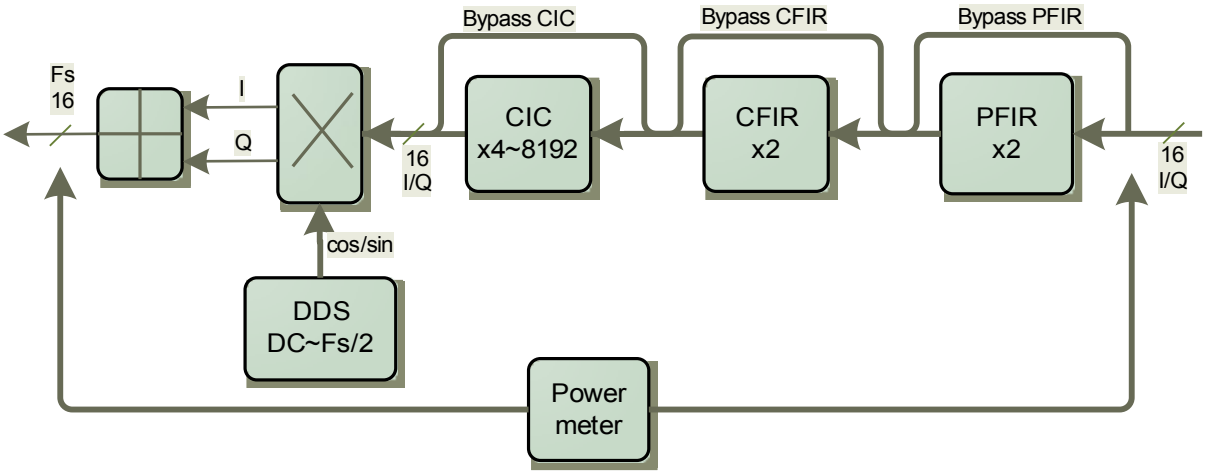

Figure 1. IP-DUC block diagram

Figure 1 shows the DUC structure utilizing the tuner and the interpolation filters. Bypass path provides the capability to deal with high bandwidth signal by using different combination of filters.

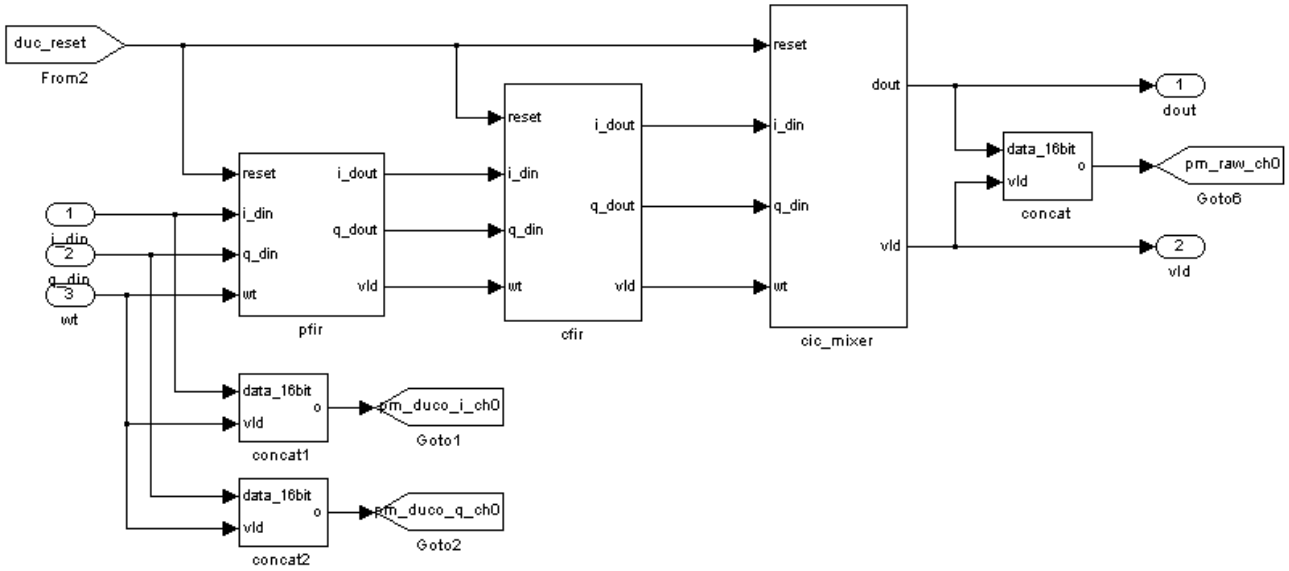

Figure 2. MATLAB/Simulink project of IP-DUC

Figure 2 shows the DUC built under MATLAB/Simulink environment using Xilinx System Generator blockset. All the signal processing blocks utilize cores from Xilinx System Generator and guaranteed to be bit true and cycle true as in the FPGA hardware. The core can be integrated with the analog front-end and FrameWork logic components for the Software Defined Radio (SDR) project on X5/X6 family modules. The system is built on the COTS (Commercial Off-The-Shelf) product, providing high performance and full upgrades to the next generation hardware using the same IP core.

IP-DUC

Port Description

Signal	Size	Direction	Description
clk_1	1	In	Clock
ce_1	1	In	Clock enable; set to '1'.
duc_reset	1	In	Asynchronous reset for DUC core
duc_i_din	16	In	16 bit input I data
duc_q_din	16	In	16 bit input Q data
duc_wt	1	In	Input data write strobe
freq_tune	32	In	Tuning frequency for the tuner
freq_tune_wt	1	In	Tuning frequency write strobe
freq_delta	24	In	Delta frequency for fine tune
freq_delta_wt	1	In	Delta frequency write strobe
cic_rate	14	In	CIC filter interpolation rate; range from 4 ~ 8192
cic_rate_wt	1	In	CIC rate write strobe
cic_bstart	8	In	CIC filter outputs gain control, which specify the starting bit of the LSB.
cic_bstart_wt	1	In	CIC bstart write strobe
cfir_coef	18	In	Compensation filter (CFIR) coefficient input
cfir_coef_wt	1	In	CFIR coefficient write strobe
pfir_coef	18	In	Programmable filter (PFIR) coefficient input
pfir_coef_wt	1	In	PFIR coefficient write strobe
cfir_bstart	7	In	CFIR outputs gain control, which specify the starting bit of the LSB.
cfir_bstart_wt	1	In	CFIR bstart write strobe
pfir_bstart	7	In	PFIR outputs gain control, which specify the starting bit of the LSB.
pfir_bstart_wt	1	In	PFIR bstart write strobe
spect_inv	1	In	Spectrum inversion enable
spect_inv_wt	1	In	Spectrum inversion write strobe
bp_cic	1	In	Bypass CIC filter
bp_cfir	1	In	Bypass CFIR
bp_pfir	1	In	Bypass PFIR
ovflo_rd	1	In	CIC, CFIR, PFIR overflow read strobe
pmeter_acc_pts	5	In	Power meter accumulate points
pmeter_src_sel	12	In	Power meter source select
duc_dout	16	Out	DUC output
duc_vld	1	Out	DUC output valid
ovflo	3	Out	Overflow signal
ovflo_alert	1	Out	Overflow alert
pmeter_dout	32	Out	Power meter data

Table 2. I/O port table

IP-DUC

Standard Features

Inputs	
Input Ch. Num.	1 (I/Q)
Input Format	16-bit, 2's complement, I/Q
Input Rate	Fs/2 to Fs/32768
Outputs	
Output Ch. Num.	1
Output Format	16-bit, 2's complement, real
Output Rate	250 MHz maximum @ 250 MHz clock *
Channel Tuning	
Tuning Range	DC to Fs/2
Tuning Resolution	Fs/2^32
CIC Filter	
Stage	4
Differential Delay	2
Interpolation Rate	4 to 8192; programmable
Compensation Filter	
Taps	20; programmable
Taps Resolution	18 bit
Programmable Filter	
Taps	80; programmable
Taps Resolution	18 bit
Other	
Bypass Filters	Available for CIC, CFIR, PFIR
Spectral Inversion	Available
Gain Range	0 to 60 dB
Overflow Indicator	Available after each filter
Power Meter	Available for DUC input/outputs

* Note: Higher output rate can be achieved by increasing the clock of the core.

Performance	
SFDR	> 115 dB (16 bit input)
S/N	Up to 90 dB

Device Utilization		
Element	FPGA Resource	Virtex-5 SX95T
FF	7396	12%
LUT	4632	7%
DSP48E	72	11%
BlockRAM	30	12%

IP-DUC

IMPORTANT NOTICES

Innovative Integration Incorporated reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Innovative Integration's terms and conditions of sale supplied at the time of order acknowledgment.

Innovative Integration warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with Innovative Integration's standard warranty. Testing and other quality control techniques are used to the extent Innovative Integration deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Innovative Integration assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Innovative Integration products. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Innovative Integration does not warrant or represent that any license, either express or implied, is granted under any Innovative Integration patent right, copyright, mask work right, or other Innovative Integration intellectual property right relating to any combination, machine, or process in which Innovative Integration products or services are used. Information published by Innovative Integration regarding third-party products or services does not constitute a license from Innovative Integration to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Innovative Integration under the patents or other intellectual property of Innovative Integration.

Reproduction of information in Innovative Integration data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice.

Innovative Integration is not responsible or liable for such altered documentation. Resale of Innovative Integration products or services with statements different from or beyond the parameters stated by Innovative Integration for that product or service voids all express and any implied warranties for the associated Innovative Integration product or service and is an unfair and deceptive business practice. Innovative Integration is not responsible or liable for any such statements.

For further information on Innovative Integration products and support see our web site:

www.innovative-dsp.com

Mailing Address: Innovative Integration, Inc.

2390A Ward Avenue, Simi Valley, California 93065

IP-DUC