

IP-DDC128



v1.0

128 Channel Digital Downconversion Core for FPGA

FEATURES

- 128 individually tuned DDC channels
- 16 bit 200MHz input
- Tuning resolution $F_s/2^{32}$
- SFDR 96 dB for 16 bits input
- Decimation range from 512 to 8192
- FFT channelizer
- Programmable 20 tap FIR (18 bit coefficient)
- Programmable 80 tap FIR (18 bit coefficient)
- Up to 60 dB gain
- Clock/sync bus for multi-module synchronization
- Test sine wave generator (SFDR 100dB)
- Overflow indicator
- DC remover
- Power meter (-77dBm ~ 13dBm)
- Supports Xilinx Virtex5 FPGA
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Digital Receivers
- Image Processing
- Spectral Analysis

IMPLEMENTATION SUPPORT

- MATLAB/Simulink model
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

HARDWARE SUPPORT

- Innovative X5 family of XMC Modules



DESCRIPTION

The IP-DDC128 core has 128 output channels of digital down-conversion (DDC). As a flexible front-end to receivers and imaging devices, this core implements the frequency translation for baseband signal recovery as FPGA firmware.

The DDC is composed of a resampled polyphase filter bank and a multiplexed DDC. The resampled polyphase filter bank splits the single wideband input data stream into 512 channel output bands equally spaced in frequency. Each channel delivers an oversampled data rate of $F_s/128$. The passband between adjacent channels overlap sufficiently so that the entire signal band is covered and further fine tune stage can slice any part of band. Out of these 512 channels 128 channels are selected by a coarse tuning function based on the programmed tuning word. Fine tuning and further decimation are performed in the DDC stage. In the DDC stage each channel has its own tuning frequency, filtering, and gain control. The overall filter response can have channel bandwidth up to $F_s/512$, and channel rejection up to 80dB. For 16 bit inputs the core has a SFDR over 96dB. Gain adjustment is allowed after each decimation filter, and an overflow indicator is provided at each point to prevent overflow. A power meter is attached to the front-end ADC raw data or the DDC output data, which allows the user to monitor both the wideband input power and the narrowband output power. A DC remover is placed at the end of the data path to remove any DC offsets present in the ADC input and in the computation process of the DDC due to truncation and asymmetric rounding.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and consumes about 40% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The testbench is bit-true, cycle-true for device simulation.

Source is available for purchase.

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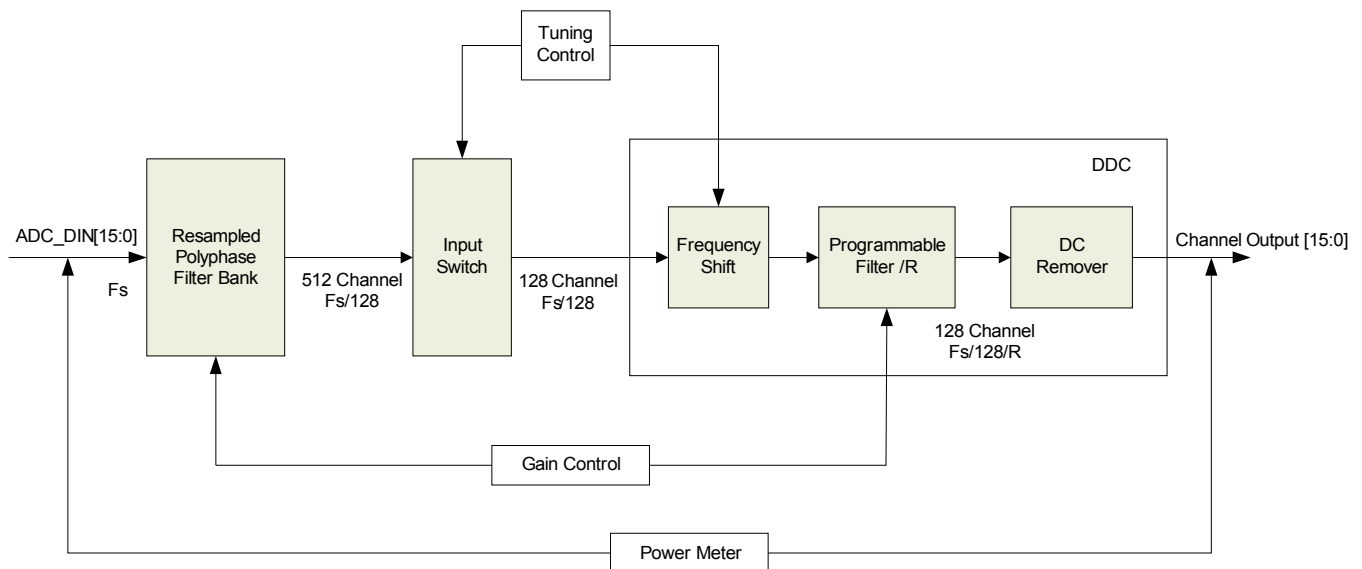
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IP-DDC128

ORDERING INFORMATION

Product	Part Number	Description
IP-MDDC128	58015	IP core for 128 independent DDC channels, netlist version, Virtex SX95T target

Block Diagram



Design Example: 128 Channel GSM DDC

As an example, a 128 channel GSM DDC is designed. The design specifications are: input data rate 138.6666MHz, channel output data rate 270.832KHz, channel spacing 200KHz, passband edge 80KHz, stopband edge 100KHz, and stopband attenuation 80dB.

1. The channelizer output response is shown in Figure 1. The channel output data rate is $F_s/128=1.083\text{MHz}$, the passband ripple is within 1dB, and the channel rejection is 80dB. The filter bank output is shifted to baseband and sent to the DDC for fine tuning further decimation.

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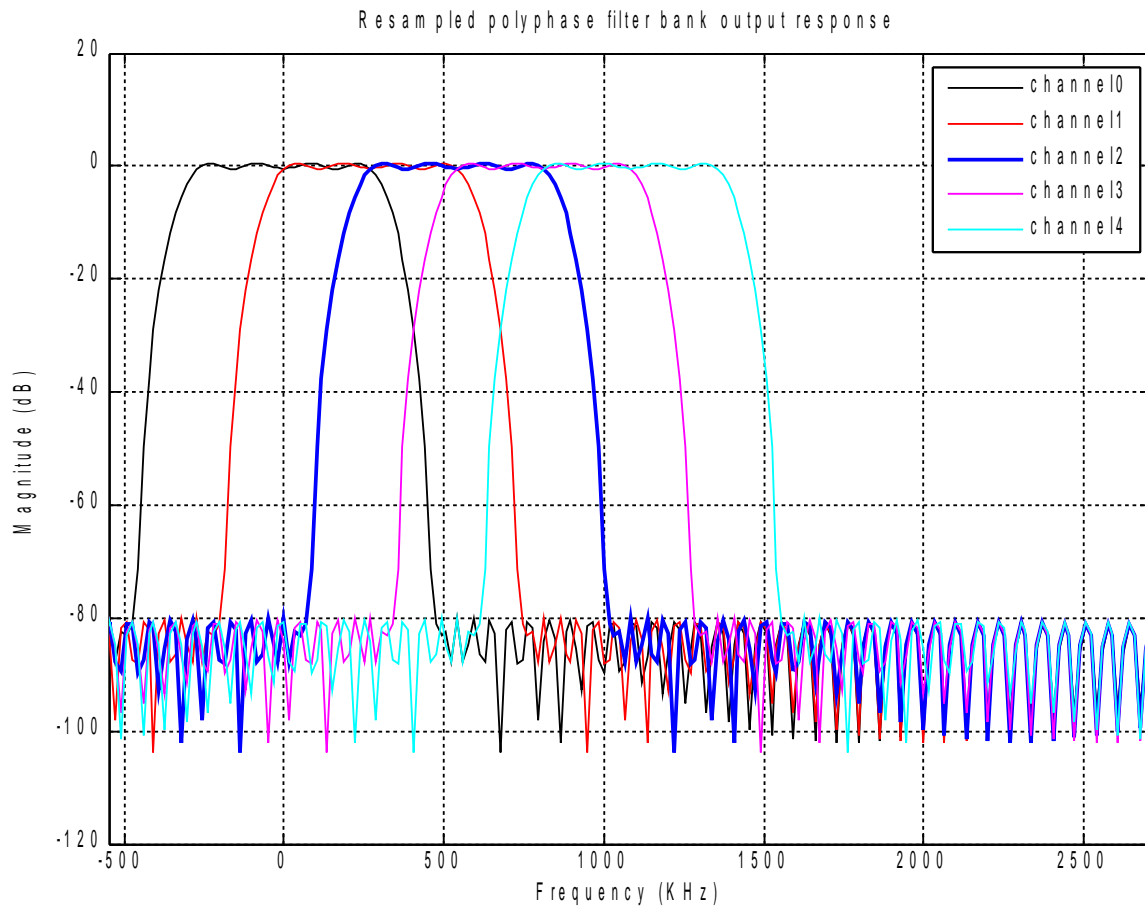


Figure 1. Polyphase filter bank output response

2. The filter response for the DDC stage is shown in Figure 2. The blue curve is the baseband channelizer output response. The dark green curve is the cascaded channelizer and decimate by 2 PFIR1(20 taps) output response. After PFIR1 the data rate becomes $F_s/128/2=541.664\text{KHz}$, and the passband edge is at 80KHz. A second PFIR with 80 taps is placed after PFIR1 to reduce the stopband to 100KHz and decimate the data rate by another factor of 2. The final filter response is shown as the red curve. Table 1 shows the overall DDC performance.

Figure 2. Overall filter response.

IP-DDC128

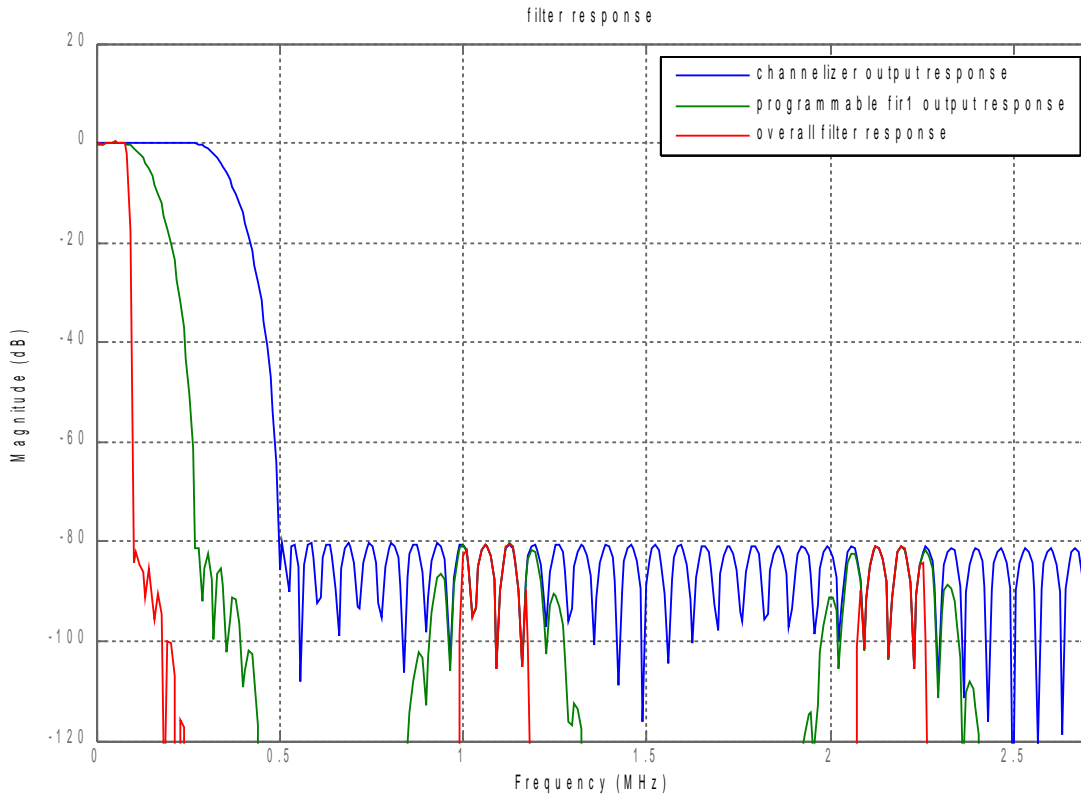


Table 1. DDC design example for GSM Digital Down Receiver

Total decimation rate	512
Fs_in	138.6666MHz
Fs_out	270.832KHz
Passband edge	80KHz
Stopband	100KHz
Passband Ripple	Within 0.4dB
Channel Rejection	80dB

Port Descriptions

Signal	Size	IO	Description
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SYST_CLK	1	I	System clock for the design. All the design operates on rising edge of SYST_CLK.
RESET	1	I	IP synchronous reset. Reset active level is high (SCLR=1).
ADC_DIN	16	I	Real input of the IP (k ranging from 0 to 3). Signed 16 bits 2's complement format. Sampled by the IP when ADC_K_WT=1.
ADC_WT	1	I	Valid signal for input ADC_DIN. Active level high.
RUN	1	I	Data streaming start signal. Active level high. Should be asserted after the IP configuration is done.
CHZ_SCALE_SCH	10	I	Programming bus for the FFT scaling schedule.
TUNING_WORD	32	I	Programming bus for the Frequency Shift unit of channel i. Computed and formatted by the IP Driver.
CHANNEL_NUM	7	I	Channel number. Used to specify the channel number for each above programmable bus.
TUNING_WORD_WT	1	I	Valid signal for TUNING_WORD. Active level high.
CFIR_BSTART	5	I	Programming bus for CFIR gain control. Computed and formatted by the IP Driver.
PFIR_BSTART	5	I	Programming bus for PFIR gain control. Computed and formatted by the IP Driver.
CFIR_COEF_DATA	18	I	Programming bus for the CFIR coefficient load. Computed and formatted by the IP Driver.
CFIR_COEF_WT	1	I	Valid signal for CFIR_COEF_DATA. Active level high.
PFIR_COEF_DATA	18	I	Programming bus for the PFIR coefficient load. Computed and formatted by the IP Driver.
PFIR_COEF_WT	1	I	Valid signal for PFIR_COEF_DATA. Active level high.
PFIR_RATE	10	I	Programming bus for the PFIR decimation rate.
PMETER_SRC_SEL	9	I	Programming bus for the power meter source select
PMETER_ACC_PTS	5	I	Integration points for the power meter accumulator.
DOUT_I	16	O	Data output. Signed 16 bits 2's complement format.
DOUT_Q	16	O	Data output. Signed 16 bits 2's complement format.
VD	1	O	Valid signal for output DOUT_I and DOUT_Q. VD is active high.
CHAN_OUT	7	O	Output channel number used to specify the channel number of the output data.
OVFLO	3	O	Overflow indicator for each decimation filter. Active level high.
PMETER_DOUT	16	O	Power meter output.

IP-DDC128

Standard Features

Inputs	
Inputs	1
Input Format	16-bit, 2's complement, real
Sample Rate	200 MHz maximum
Outputs	
Outputs	128
Output Type	Complex I & Q
Output Format	16-bit, 2's complement
Output Rate	Fs/512 to Fs/8192
Channel Tuning	
Tuning Range	DC to Fs/2
Tuning Resolution	Fs/2 ³²
Gain	
Range	0 to 60 dB
Compensation Filter	
Taps	20
Taps Resolution	18 bit
Programmable Filter	
Taps	80
Taps Resolution	18 bit

Performance	
SFDR	96 dB (16 bit input)
S/N	Up to 80 dB

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
DSP48E	313	48%
LUT	26.2K	44%
FF	23.8K	40%
BlockRAM	104	42%

IP-DDC128

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