

IP-OFDM-LTE-TX

LTE Downlink Transmitter OFDM Component IP Core

FEATURES

- Support for 128, 256, 512, 1k, and 2k iFFT sizes to address variable bandwidths from 1.4 MHz to 20 MHz.
- Variable cyclic prefix length for support of “normal” and “extended” cyclic prefix modes.
- Each I and Q coordinates specified with 9 bits precision support BPSK, QPSK, 16QAM, and 64QAM modulation schemes with less than 0.5% quantization error.
- Maximum iFFT/FFT conversion time less than 44 us with system clock at 250 MHz
- Programmable RRC filter with user defined 16 bit coefficients
- Variable time domain windowing with user programmable window length and window tails
- Bit-true, cycle-true MATLAB and Modelsim model

APPLICATIONS

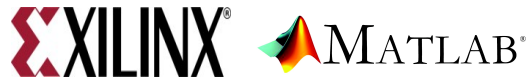
- LTE eNodeB PHY layer development
- RF IC development
- Cellular test equipment
- Security surveillance equipment

IMPLEMENTATION SUPPORT

- MATLAB/Simulink model
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules



DESCRIPTION

IP-OFDM-LTE-TX is used to accelerate the hardware implementation of the 3GPP LTE physical layer on Virtex-5 and FPGAs. This core implements that end vector-signal generator for transmit functions for cyclic prefix generation, signal generation, and windowing used in LTE applications.



The IP-OFDM-LTE-TX core provides a flexible I/Q vector signal generator for OFDM systems. The channel bandwidth, signal modulation, prefix type, window size and output shaping filter are all programmable. This allows the core to be used in test and measurement applications to evaluate user end equipment and sub-systems.

An LTE baseband signal generation test system is available using this core that simulates eNodeB transmit operation with channel impairments. The test system generates baseband signals using BPSK, QPSK, and QAM modulations through a programmable channel model that are output real-time using an Innovative X5-TX transmitter module. Pre-programmed channel models for LTE pedestrian, vehicular and high-speed train usage are provided. These standard channel models are complemented by programmable channel impairments for noise level, fading environment, Doppler and frequency offset, allowing test engineers to evaluate system performance under diverse conditions.

The core is targeted at the Xilinx Virtex-5 SX95T FPGA and consumes about 19% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex-5 or Virtex-6 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The testbench is bit-true, cycle-true for device simulation.

Source is available for purchase.

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03/29/11

IP-OFDM-LTE-TX

Ordering Information

Product	Part Number	Description
IP-OFDM-LTE-TX	58029-0	Netlist version bundled with X6/X5 boards
	58029-1	Netlist Version Only
	58029-2	Source Code Version

Table 1. Product information

IP-OFDM-LTE-TX

Block Diagram

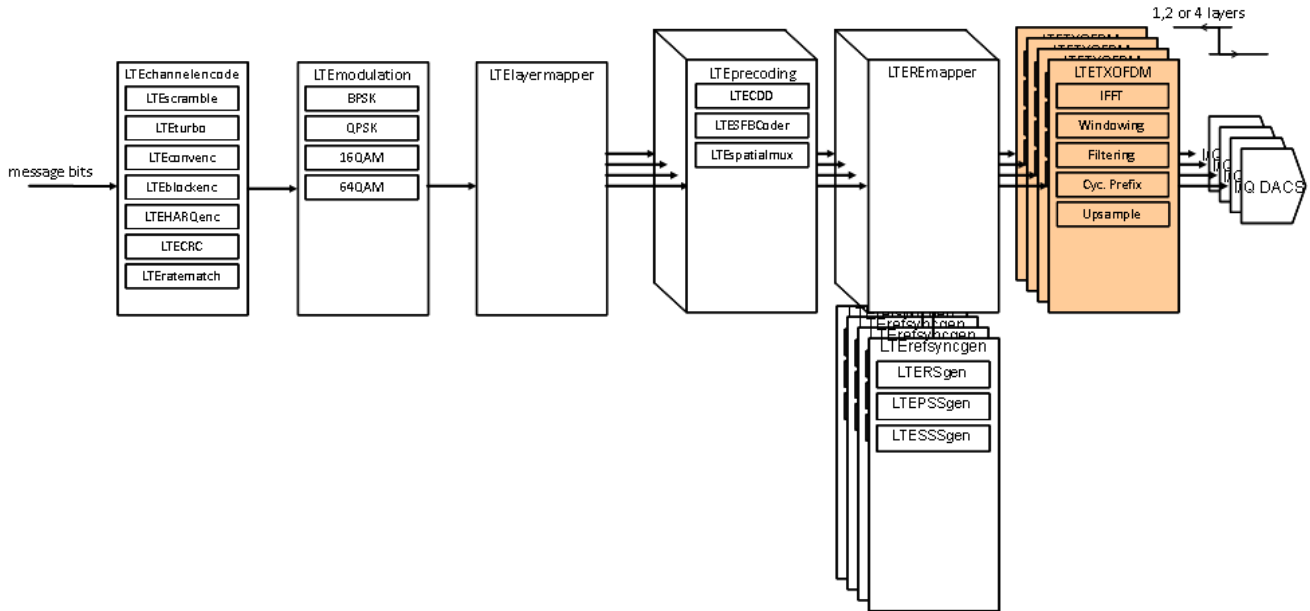


Figure 1. LTE downlink transmitter PHY layer block diagram

The above block diagram provides a generalized structure of the Innovative Integration LTE downlink transmitter reference design for both MATLAB and FPGA realizations. Flat blocks represent functions that operate independently of other layers, and solid blocks represent functions that require access to all available layers. IP-OFDM-LTE-TX supports the block highlighted with the orange color.

The block in Figure 2 takes the resulting 3-dimensional frequency-domain OFDM symbol vector and performs an IFFT. The cyclic prefix is performed by taking the last group of samples and prefixing them on the result of the IFFT. The number of samples depends on the IFFT size as well as the cyclic prefix mode and symbol index in a given slot. In each case, a varying number of extra sacrificial cyclic prefix samples can be added for the windowing process. The resulting symbol boundaries are then multiplied by the tails of the Blackman-harris window and are added to the next symbol in time. This allows for a reduced-order FIR filter to be used to meet the spectral mask. This process reduces the usable CP window at the receiver, so the window length must be kept to a minimum.

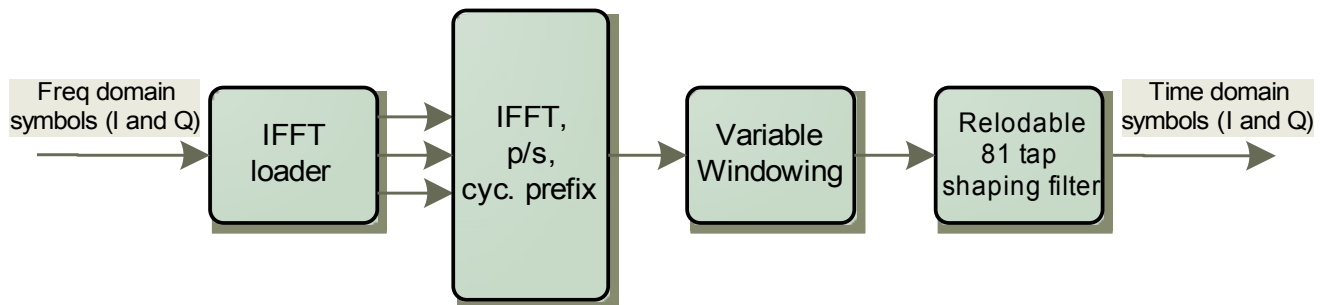


Figure 2. OFDM downlink transmitter block

IP-OFDM-LTE-TX supports various bandwidth options mentioned in LTE specification. Table 2 shows the available

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bandwidth options and corresponding iFFT sizes.

iFFT Size	Bandwidth (MHz)
128	1.5
256	3
512	5
1024	10
2048	15 and 20

Table 2. OFDM transmitter bandwidth options

Figure 3 shows the system integration of OFDM transmitter and II X5-400M using II board support package (BSP) and Xilinx System Generator in MATLAB/Simulink environment.

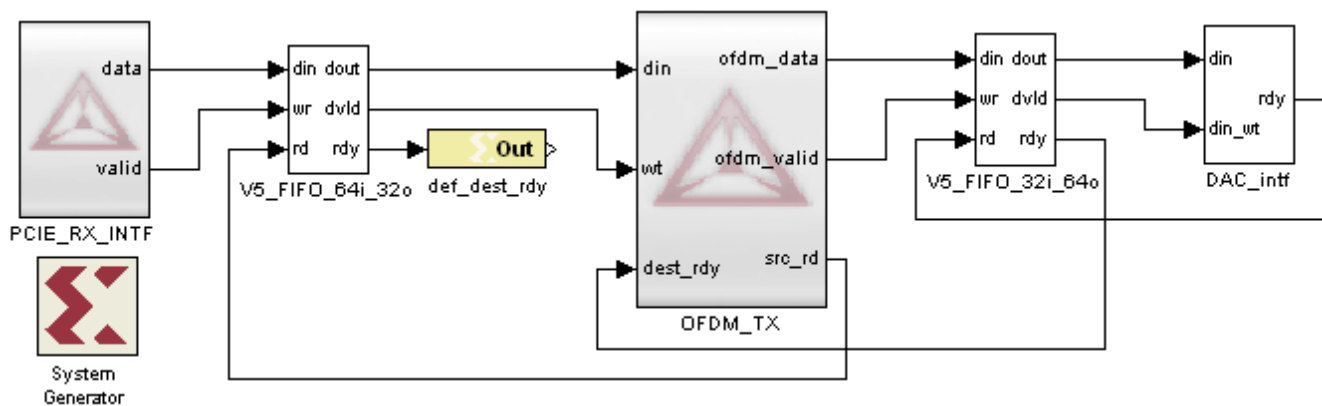


Figure 3. MATLAB/Simulink system integration of OFDM transmitter

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MATLAB Model - LTE PHY Downlink Transmit (eNodeB) Signal Generator

Features

- Normal/Extended cyclic prefix
- PDSCH modulation schemes (QPSK, 16QAM, 64QAM)
- Cell ID settings
- SNR level settings
- Frequency offset and timing delay offsets
- Bandwidth selection from 1.4 MHz to 20 MHz
- Channel Model

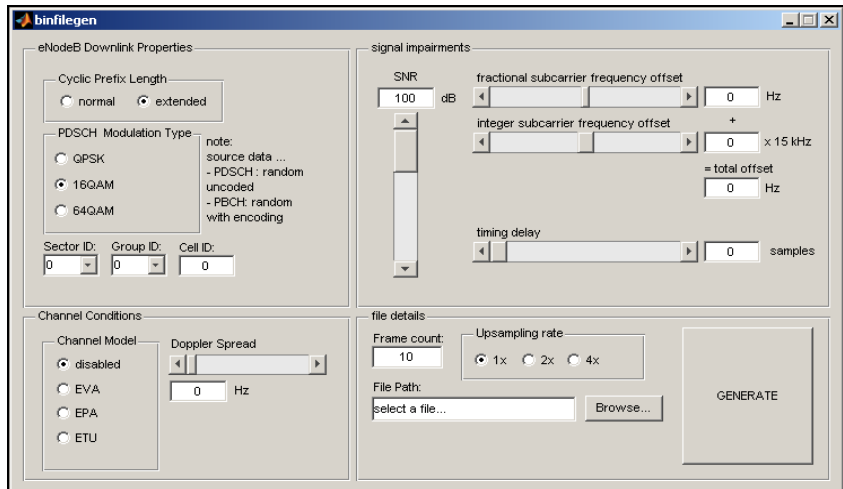


Figure 4. MATLAB software model for simulation and testing

Port Description

Signal	Direction	Description
sys_clk	Input(Boolean)	System clock for the design. All the design operates on rising edge of SYS_CLK.
reset	Input(Boolean)	IP synchronous reset. Reset active level is high (SCLR=1).
cp_length	Input(UFIX_11_0)	Provides cyclic prefix length size for the current OFDM symbol
cp_length_we	Input(Boolean)	Cyclic prefix length write enable signal
iFFT_size	Input(UFIX_5_0)	Provides the iFFT size for the OFDM symbol. The value of the iFFT length is $\log_2(\text{point size})$
iFFT_size_we	Input(Boolean)	When asserted, loads the point size for the OFDM symbol
iFFT_re_in	Input(FIX_9_0)	9 bit real input (I) for the iFFT engine
iFFT_im_in	Input(FIX_9_0)	9 bit Imaginary input (Q) for the iFFT engine
iFFT_din_valid	Input(Boolean)	Data valid signal for real and imaginary input

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Signal	Direction	Description
iFFT_wr_error	Output(Boolean)	Signal indicating error in writing the OFDM symbol
iFFT_loader_rdy	Output(Boolean)	Signal indicating iFFT loader ready to accept new OFDM symbol
iFFT_dest_rdy	Input(Boolean)	Signal indicating Destination is ready to accept the output of the iFFT engine
iFFT_re_out	Output(FIX_16_0)	Real (I) output from the OFDM transmit IP core
iFFT_im_out	Output(FIX_16_0)	Imaginary(Q) output from the OFDM transmit IP core
iFFT_dout_valid	Output(Boolean)	Data valid signal
iFFT_cp_valid	Output(Boolean)	Cyclic prefix valid signal
coef_data	Input(FIX_16_0)	Filter coefficient data
coef_wt	Input (Boolean)	Filter coefficient data write enable
win_data	Input(FIX_16_0)	Window sample data
win_data_wt	Input(Boolean)	Window data write enable
win_bypass	Input(Boolean)	Bypass windows function
filter_bypass	Input(Boolean)	Bypass pulse shaping filter

Table 3. IP-OFDM-LTE-TX I/O Ports

Resource Requirements

FPGA	Slice LUTs	Slice Registers (FFs)	BRAMs	DSP48Es	Maximum Clock (MHz)
Virtex-5-SX95T-1	10665 (18%)	11273 (19%)	7 (2%)	114 (17%)	250
Virtex-6-Lx240T-1	10665 (4%)	11273 (4%)	8 (1%)	114 (14%)	250

Table 4. Xilinx FPGA resource usage

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Example Implementation

In this example, IP-OFDM-LTE-TX is implemented on Xilinx Virtex-5 SX95T on Innovative Integration X5-400M board. The output signal of different configurations are shown in Figure 5 and 6.

Figure 5 shows the bandwidth plot for 10 Mhz bandwidth without windowing and filtering.

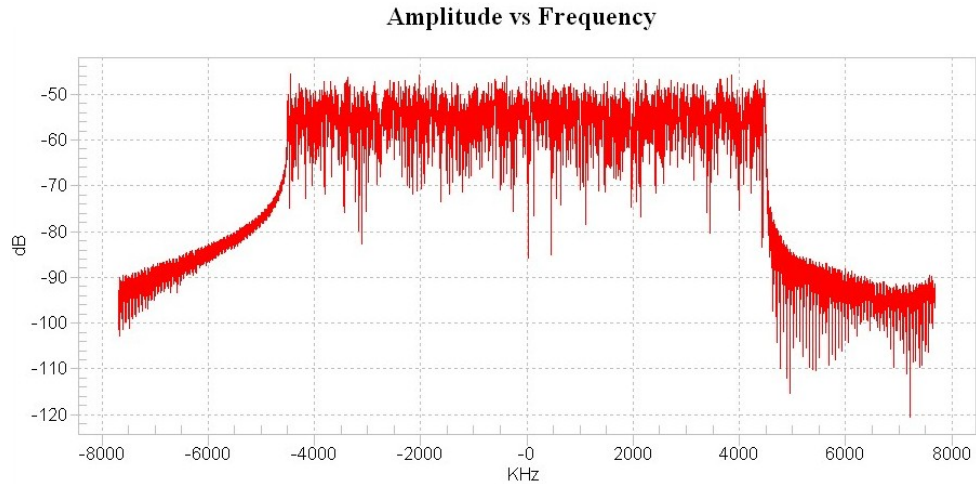


Figure 5. Bandwidth plot without filtering and windowing

Figure 6 shows the bandwidth plots for the 10 Mhz bandwidth with filter and 8 sample windowing

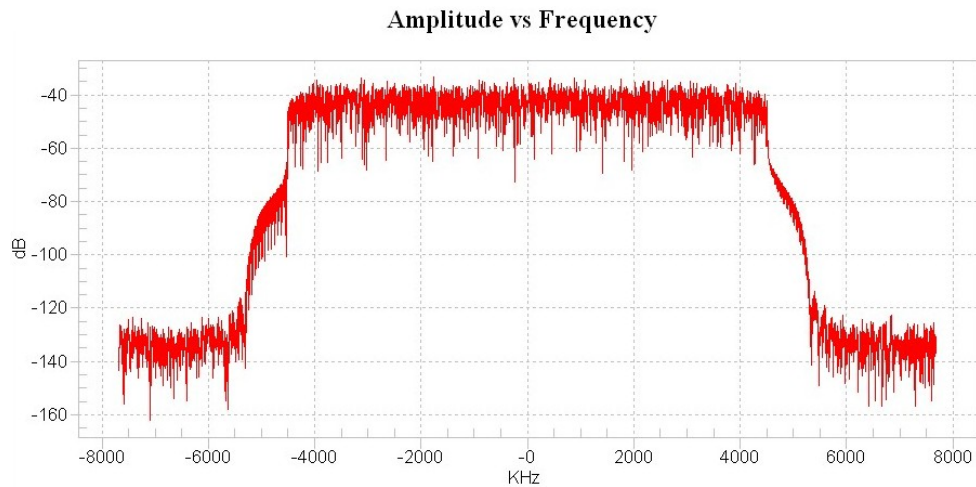


Figure 6. 10 MHz Bandwidth plot with the filter

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