IP-PSK-DEMOD

v1.3

BPSK, QPSK, 8-PSK Demodulator for FPGA

FEATURES

- Multi-mode Phase Shift Keying demodulator supporting BPSK, QPSK, 8-PSK
- Symbol rate from 1 KSPS to 18.5 MSPS
- Matched filtering with 63 taps, programmable root-raised cosine filter
- Built-in automatic gain control (AGC)
- Data resampler with fractional delay filter using Farrow structure
- High performance Maximum Likelihood (ML) timing error detector
- Second order carrier and timing tracking loop filters with programmable loop gains
- Symbol decision with mapping table
- Preamble detection for BER calculation
- Lock detector
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Satellite communications
- Communications testing equipment
- Security and surveillance equipment

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes

Description

The IP-PSK-DEMOD core provides demodulation for phase-shift keying (PSK) data in a compact FPGA IP core. The demodulation mode is dynamically programmable for M=2, 4, or 8 phase demodulation. This core includes a matched filter, an automatic gain control (AGC), a timing recovery loop, a carrier recovery loop, symbol decision, and a preamble detector logic providing a complete PSK demodulation solution for the communication systems.

The PSK demodulator core processes 16-bit baseband In-Phase (I) and Quadrature (Q) data. The input data rate is required to be 8 times of the symbol rate. The programmable RRC filter is to eliminate inter-symbol interference (ISI). Following the RRC filter, the AGC is to maximize the dynamic range of the signal magnitude and maintain an optimal level for symbol decision. Output of the AGC is resampled by the FD filter at symbol clock, which is built inside the timing recovery loop. In the timing error detector, a Maximum Likelihood based technique is applied to achieve an asymptotically jitter free timing error estimate. The resampled I/Q data is multiplied by the NCO outputs to remove any residual carrier frequency. Finally the symbol decision component encodes the demodulated I/Q samples into 8-bit hard-coded symbols according to the user defined mapping table. Both the demodulated I/Q samples and symbols are available at the outputs simultaneously. The lock detector monitors the timing and carrier loop errors and asserts a lock signal when both accumulated errors are within the threshold during a predefined amount of time. Preamble detector finds the frame size and does BER calculation according to the known preamble information.

The core is targeted at the Xilinx Virtex-5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex-5/6 designs with the constraints and implementation control files provided.

MATLAB/Simulink simulation models for system design are provided with test vectors. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

IP-PSK-DEMOD

Ordering Information

Product	Part Number	Description
IP-PSK-DEMOD	58001-0	Netlist version bundled with X6/X5 boards
	58001-1	Netlist Version Only
	58001-2	Source Code Version

Table 1. Product information

Block Diagram

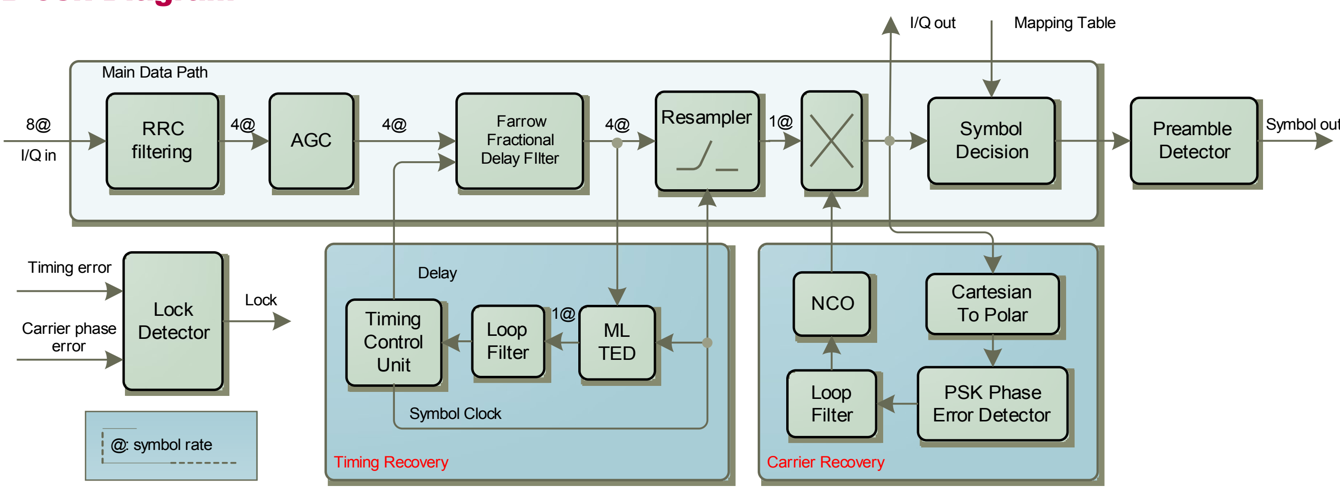

Figure 1. PSK demodulator block diagram

The RRC filter is placed as the match filter to eliminate ISI. A high performance Maximum Likelihood timing error detector (TED) is implemented to generate jitter free timing error and considered to be an optimal approach for the current digital demodulator design. Farrow structure FD filter, serving as an interpolation filter, provides intermediate data between adjacent samples for the highest SNR output. Carrier recovery loop takes one sample per symbol, detects the phase error, feeds back the error information to the sine/cosine table (or NCO) through a second order loop filter, and removes the residual carrier frequency.

As shown in Figure 1, limited by the timing error range of the timing recovery loop, the core requires the input data rate to be eight times of the symbol rate.

IP-PSK-DEMOD

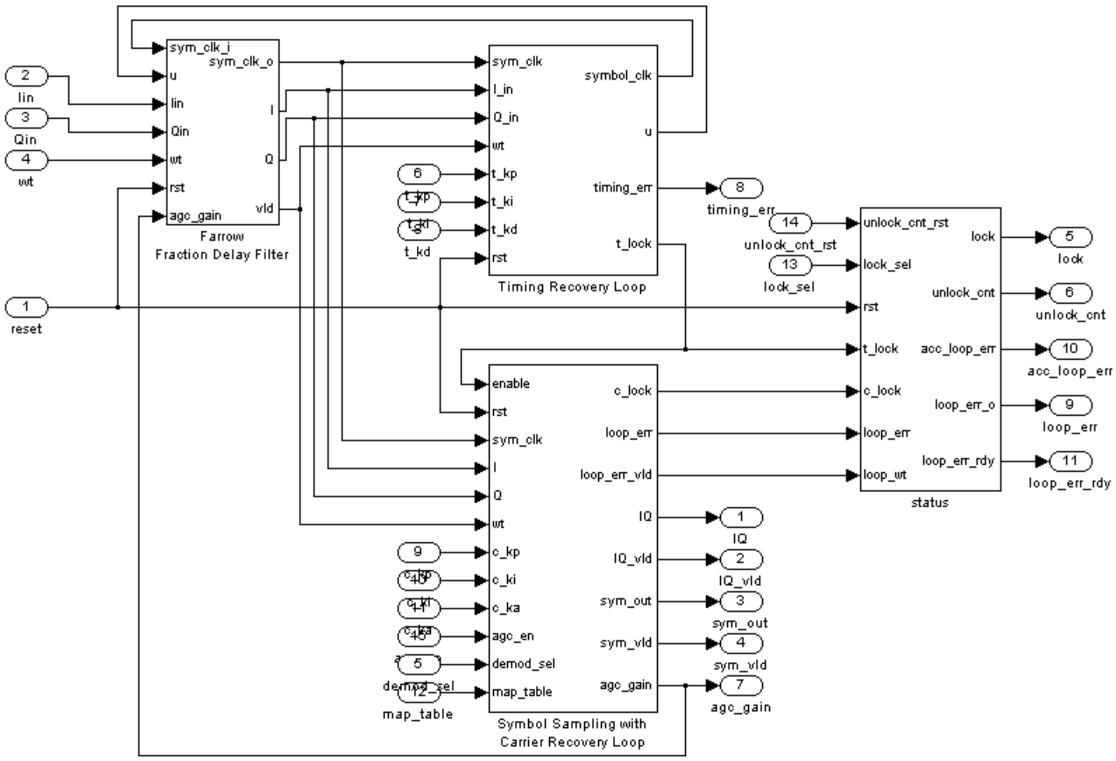

Figure 2. MATLAB/Simulink project of PSK demodulator

Figure 2 shows the PSK demodulator built under MATLAB/Simulink environment using Xilinx System Generator blockset. All the signal processing blocks utilize cores from Xilinx System Generator and guaranteed to be bit true and cycle true as in the FPGA hardware. In Figure 3, the core is integrated with the analog front end, a multichannel DDC, and FrameWork logic components for the Software Defined Radio (SDR) project on X5-210M. This system is built on the COTS (Commercial Off-The-Shelf) product, providing high performance and full upgrades to the next generation hardware using the same IP core.

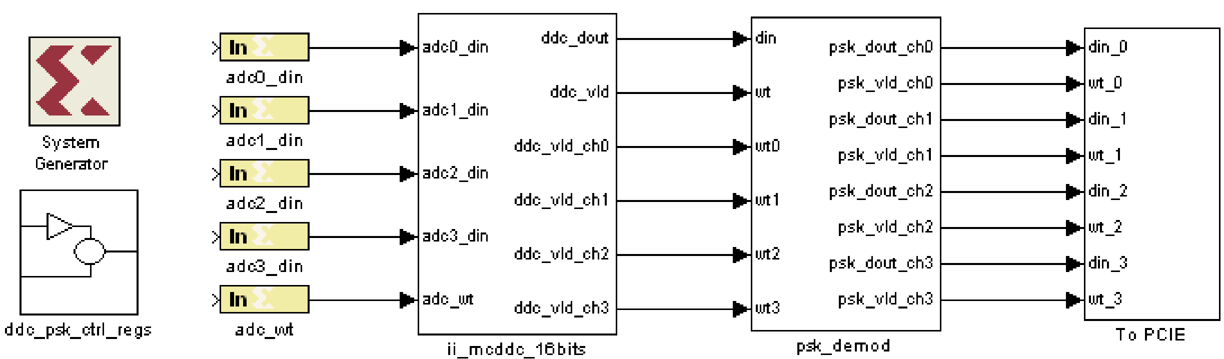

Figure 3. MATLAB/Simulink system integration of DDC and PSK demodulator

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Bit Error Rate (BER) Performance

The BER performance of the PSK demodulation core versus Eb/No is shown below. The data is measured by the embedded preamble detector (PD), which looks for the preamble in the signal, compares with the given preamble information, and calculate the BER. Solid and dashed curves are theoretical BER values, and markers are BER measurements under different noisy environment. BER of BPSK signal is right on the theoretical curve; BER of QPSK and 8-PSK signal are within 1 dB from the curve. The BER will be improved after Forward Error Correction (FEC).

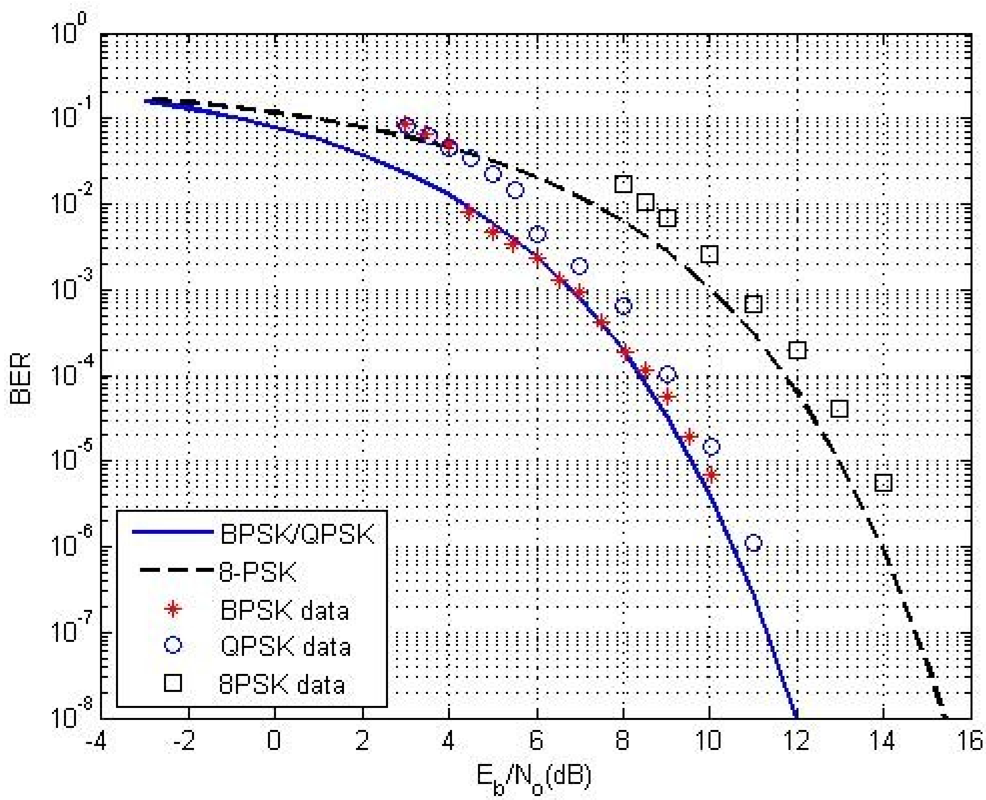

Figure 4. BER versus Eb/No. The solid and dash lines are theoretic curve from [Wikipedia](#).

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Port Description

Signal	Size	Direction	Description
clk_1	1	In	Clock; 200 MHz or faster.
ce_1	1	In	Clock enable; set to '1'.
psk_reset	1	In	Asynchronous reset for PSK core, active high
psk_reset_wt	1	In	Write strobe of psk_reset
demod_sel	3	In	Demodulation type selection
demod_sel_wt	1	In	Write strobe of demod_sel
i_din	16	In	Real data input
q_din	16	In	Imaginary data input
iq_wt	1	In	Write strobe of input I/Q data
t_kp	8	In	Proportional gain of timing recovery loop, default=6.
t_ki	8	In	Integral gain of timing recovery loop, default=70.
t_kd	8	In	Derivative gain of timing recovery loop, default=14.
t_k_wt	1	In	Write strobe of timing loop gains
c_kp	8	In	Proportional gain of carrier recovery loop, default=3.
c_ki	8	In	Integral gain of carrier recovery loop, default=4.
c_k_wt	1	In	Write strobe of carrier loop gains
rrc_coef	16	In	RRC filter coefficient input
rrc_coef_wt	1	In	Write strobe of RRC filter coefficients
map_table	24	In	Mapping table for symbol decision
map_table_wt	1	In	Write strobe of map_table
agc_en	1	In	AGC enable
agc_en_wt	1	In	Write strobe of agc_en
iq_dout	8	Out	Demodulated I/Q data; bit 15..8 => I; bit 7..0 => Q
iq_vld	1	Out	Valid strobe of iq_dout
sym	8	Out	Hard coded symbol output
sym_vld	1	Out	Valid strobe of symbols
agc_gain	4	Out	AGC gain
psk_err	8	Out	PSK carrier loop error
psk_err_rdy	1	Out	Ready signal of psk_err
lock	1	Out	Lock signal
unlock_cnt	6	Out	Unlock counter
pd_rst	1	In	Preamble detector reset
bs_err_cnt_sel	1	In	Select bit/symbol error
derotate_en	1	In	Enable symbol derotation according to the given preamble information
preamble	27	In	Preamble information
frame_size	16	Out	Frame size between two preambles
preamble_cnt	16	Out	Preamble counter output
bs_err_cnt	16	Out	Bit/symbol error counter output

Table 2. I/O port table

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Example Implementation

The example design includes four channels of independent DDCs and IP-PSK-DEMOD4 core on Virtex-5 SX95T. The PSK signal of carrier at 5 MHz is from Agilent E4433B; AWGN noise and adjacent channels are generated by X5-400M. The noise signal is filtered and combined with the PSK test signal as shown in Figure 6. After down-conversion and demodulation, the I/Q is plotted in Figure 7 and the BER is 6.48e-4.

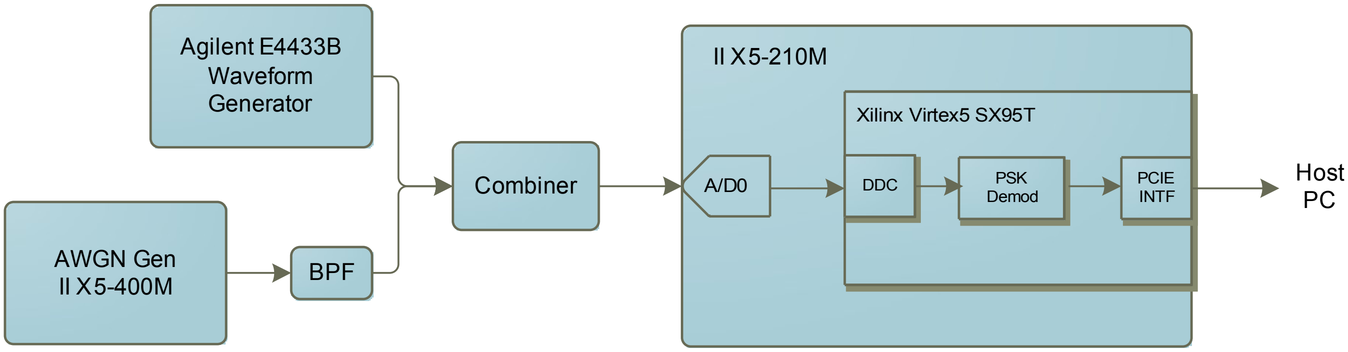

Figure 5. IP core implementation on X5-210M and the test environment

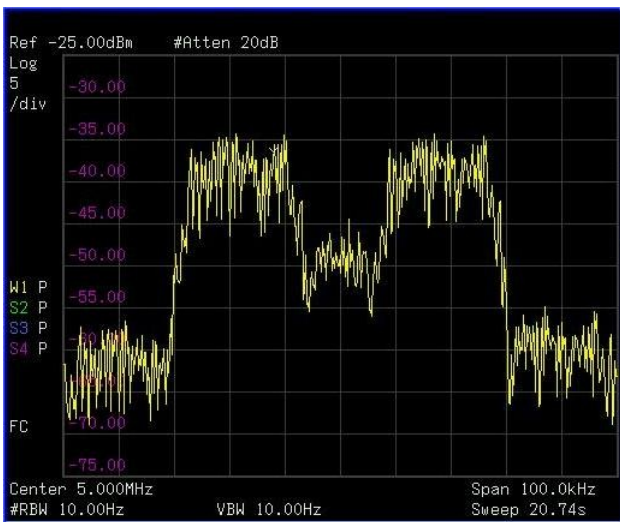

Figure 6. Fcarrier=5 MHz, 10KHz symbol rate QPSK signal with two adjacent channels. Channel interval is 4 KHz or less.

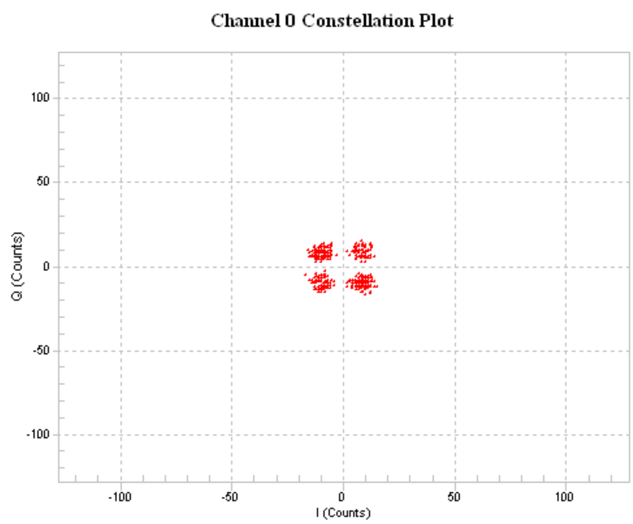

Figure 7. Demodulated QPSK constellation, BER=6.48e-4.

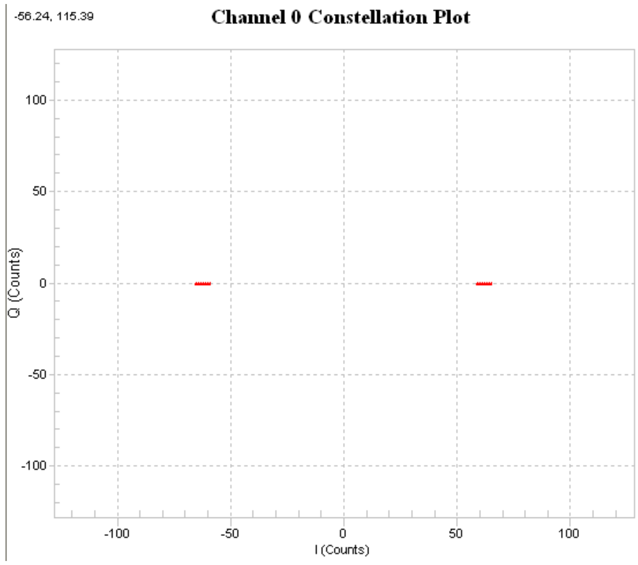

Figure 8. Demodulated BPSK constellation without noise

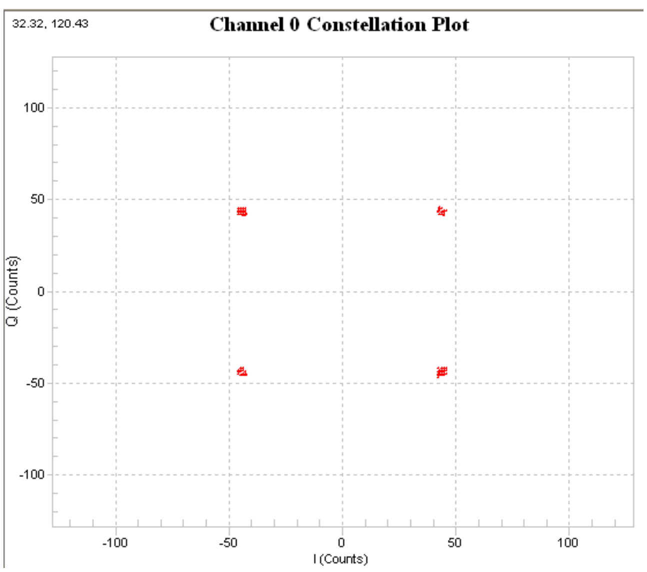

Figure 9. Demodulated QPSK constellation without noise

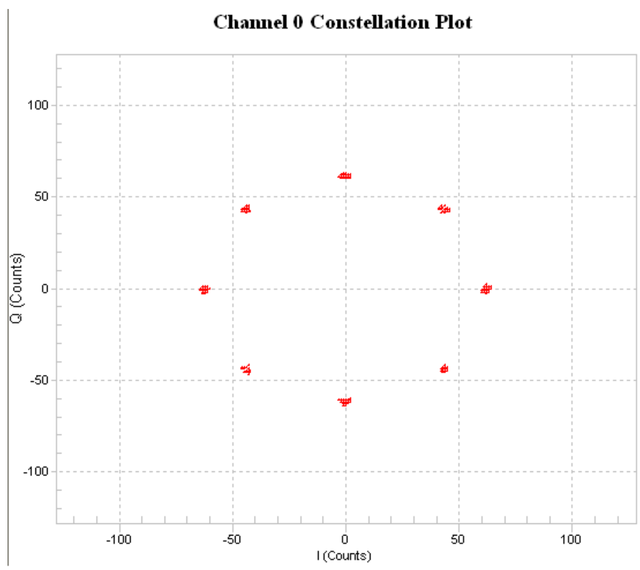

Figure 10. Demodulated 8-PSK constellation without noise

IP-PSK-DEMOD

Standard Features

Inputs			
Input Channel Number	1		
Input Format	16-bit, 2's complement, complex interleaved		
Input Rate	**Symbol rate x8**		
Outputs			
Output Channel Number	1		
Output Format	Demodulated I/Q: 8-bit, 2's complement Symbol: 8-bit, unsigned		
Demodulation			
Type	BPSK, QPSK, 8-PSK		
Symbol Rate	1 KSPS to 18.5 MSPS @ 250 MHz clock *		
Timing Error Range	+- 1% of symbol rate		
Frequency Error Range	+- 5% of symbol rate		
Acquisition Time	< 850 ms (QPSK at Eb/No = 5.5 dB, symbol rate = 10 KSPS)		
	BPSK	QPSK	8-PSK
Minimum Eb/No	5.5 dB	6 dB	11 dB
Root Raised Cosine Filter	63 taps, programmable in ini file		
Power Consumption	0.206 Watt		

* Note: Higher symbol rate can be achieved by increasing the clock or reducing timing loop latency.

Device Utilization		
Element	FPGA Resource	Virtex-5 SX95T
FF	12403	21.1%
LUT	8490	14%
DSP48E	181	28%
BlockRAM	32	13%

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IMPORTANT NOTICES

For further information on Innovative Integration products and support see our web site:

www.innovative-dsp.com

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