IP-PSK-DEMOD

v1.2

BPSK, QPSK, 8-PSK Demodulator for FPGA

FEATURES

- Multi-mode Phase Shift Keyed Demodulator supports BPSK, QPSK, 8-PSK
- Symbol rates to over 1Msps
- Matched filtering with Root Raised Cosine Filter
- Data resampler with Fractional Delay Filter using Farrow Structure
- Second Order Carrier and Symbol Tracking Loop Filters
- Automatic Gain Control (AGC) 0 to 42 dB
- Lock Detector
- Symbol Decision
- Flow control
- Supports Xilinx Virtex5 FPGA
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Satellite receivers
- Communications testing
- Surveillance

IMPLEMENTATION SUPPORT

- MATLAB/Simulink files
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

DESCRIPTION

The IP-PSK-DEMOD core provides demodulation for Phase Shift Keyed (PSK) data in a compact FPGA IP core. The demodulation mode can be dynamically programmable for M=2, 4, or 8 phase demodulation. This core also includes AGC, matched filtering, carrier recovery, timing recovery, and symbol decision logic providing a complete PSK demodulation solution for communication systems.

The PSK demodulator processes 16 bit baseband In-Phase(I) and quadrature(Q) data. The input data rate is 8 times symbol rate. The main data path includes a matched filter using Root Raised Cosine filter (RRC), AGC, resampler using Fractional Delay (FD) Filter and a complex multiplier. The coefficient reloadable RRC filter is used as matched filter. Following the RRC filter the AGC is used to maximize the dynamic range of the signal magnitude and maintain an optimal output sample level for symbol decision. Outputs of the AGC is resampled by the FD filter at symbol clock, which is built by the timing recovery loop. In the timing loop error detector Maximum Likelihood based spectrum analysis technique is provided to achieve an asymptotically jitter free timing error estimate. The resampled I/Q data is multiplied by the NCO outputs to remove any residual carrier frequency. Finally the symbol decision component encodes the demodulated I/Q samples into 3bit hard-coded symbols according to user input map table. Both demodulated I/Q samples and hard-coded symbols are available at the outputs. The lock detector monitors the timing and carrier loop errors and asserts a lock signal when both accumulated errors are within the threshold during a predefined observation time.

The core is targeted at the Xilinx Virtex5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASIC.

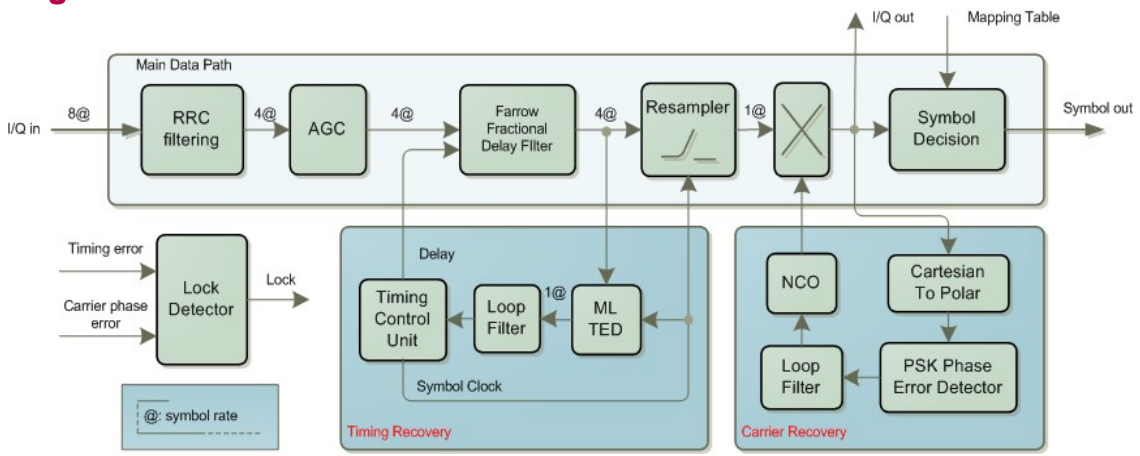
Simulation models for system design are provided as fixed point MATLAB/Simulink files. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.

IP-PSK-DEMOD

ORDERING INFORMATION

Product	Part Number	Description
IP-PSK-DEMOD	58001	IP core PSK Demodulator, netlist version, Virtex5 SX95T target

Block diagram

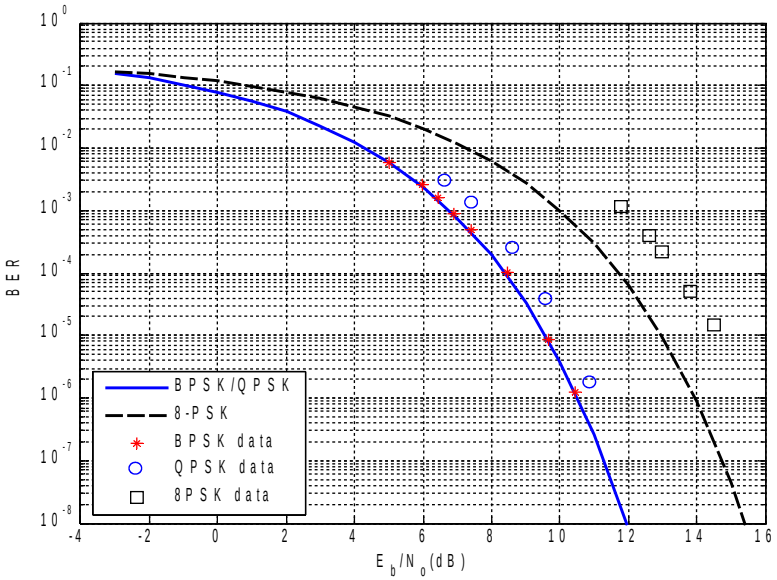


Port Descriptions

Signal	Size	IO	Description
reset	1	I	Asynchronous reset, active high.
clk	1	I	clock
i_din[15:0]	16	I	Data in.
din_wt	1	I	Data in write strobe.
q_din[15:0]	16	I	Data in.
demod_sel[2:0]	3	I	Demodulation select
rrc_bypass	1	I	RRC filter bypass
rrc_coef[15:0]	16	I	RRC coefficient
rrc_coef_wt	1	I	RRC coefficient write strobe
t_kp[7:0]	8	I	Proportional gain in the timing recovery loop filter.
t_ki[7:0]	8	I	Integral gain in the timing recovery loop filter.
t_kd[7:0]	8	I	Differential gain in the timing recovery loop filter.
c_kp[7:0]	8	I	Proportional gain in the carrier recovery loop filter.
c_ki[7:0]	8	I	Integral gain in the carrier recovery loop filter.
agc_mode[1:0]	2	I	AGC operation mode.

agc_gain[3:0]	4	I	AGC gain for fixed mode.
agc_hi_thresh[7:0]	8	I	AGC upper boundary for auto mode.
agc_lo_thresh[7:0]	8	I	AGC lower boundary for auto mode.
map_table[23:0]	24	I	Map table for symbol decision
I_dout[15:0]	16	O	N bits in phase part of the complex output
Q_dout[15:0]	16	O	N bits in phase part of the complex output
symbol_out[2:0]	3	O	Hard coded symbol output
valid	1	O	Valid output signal for channel i complex output components. Active high.
lock	1	O	lock signal.
unlock_cnt	10	O	Unlock count.

Bit-error rate (BER) Performance



Solid and dashed curves are theoretical BER values. Markers are II_PSK_demod core measurements.

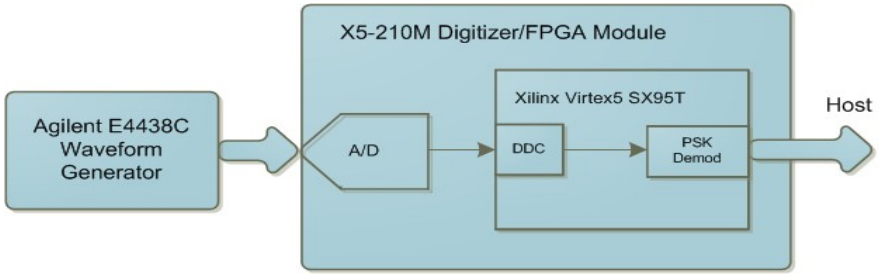
BER performance: less than 0.02dB, 1dB and 2dB compared to theoretical curves for BPSK, QPSK and 8PSK, respectively.

Minimum Eb/No for locking: 5dB for BPSK, 6.5dB for QPSK, and 12dB for 8PSK.

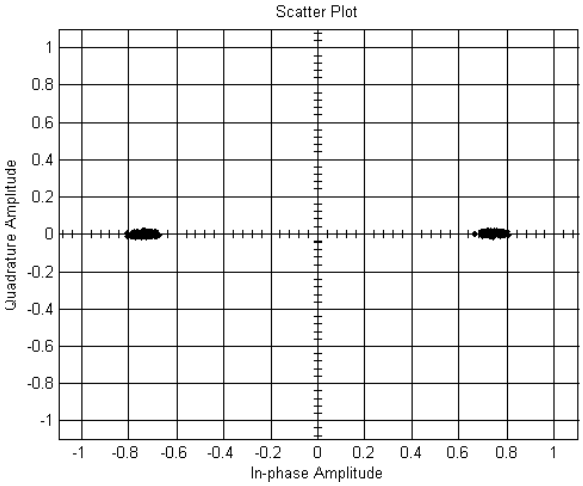
Example Implementation

In this example, a 19.2 KHz BPSK, QPSK, and 8-PSK PN9 signal is generated in Agilent E4438C. A digital downconverter and the IP-PSK DEMOD are implemented in a Xilinx Virtex5 SX95T on an Innovative X5-210M board and demodulate the symbols as I/Q outputs.

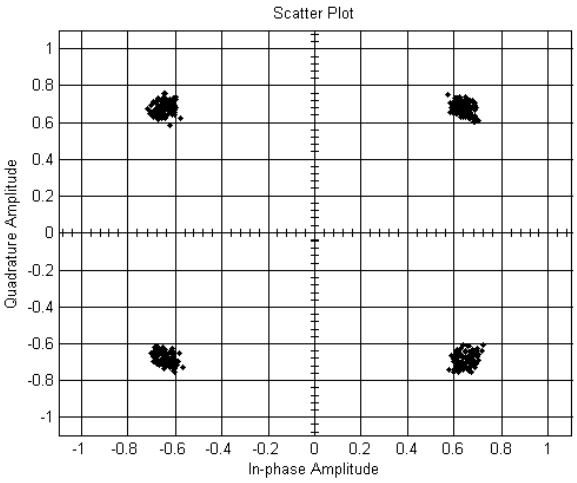
IP-PSK-DEMOD



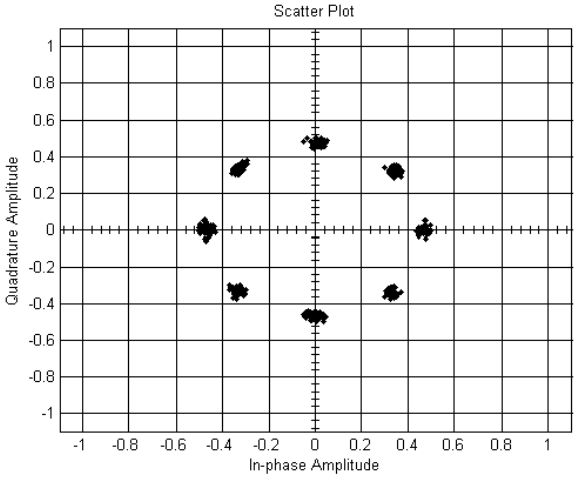
Hardware Implementation



Constellation plot of BPSK data



Constellation plot of QPSK data



Constellation plot of 8PSK data

IP-PSK-DEMOD

Standard Features

Inputs			
Inputs	1		
Input Format	16-bit, 2's complement, complex		
Outputs			
Outputs	1		
Output Format	16-bit, 2's complement, complex		
Demodulation			
Formats	BPSK, QPSK, 8-PSK		
Symbol Rate	Up to 1.4 MSPS		
Input sample rate	8 times symbol rate		
Symbol locking range	0.56% of symbol rate		
Acquisition time	Less than 50msec		
	BPSK	QPSK	8PSK
Carrier locking range	Up to 140ksps	Up to 140ksps	Up to 70ksps
Level of performance compared to theoretical	within 0.02dB	within 1dB	within 2dB
Minimum Eb/No	5dB	6.5dB	12dB
Gain Control			
Range	0 to 42 dB, auto-ranging		

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
LUT	6383	10.8%
FF	10626	18.0%
DSP48E	81	12%
BlockRAM	18	7%

IP-PSK-DEMOD

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