

# IP-PSK-DEMOD



v1.3

## BPSK, QPSK, 8-PSK Demodulator for FPGA

### FEATURES

- Multi-mode Phase Shift Keyed demodulator supports BPSK, QPSK, 8-PSK
- Symbol rates up to 1.4 MSPS
- Matched filtering with programmable Root Raised Cosine Filter
- Data resampler with Fractional Delay filter using Farrow Structure
- Second order carrier and symbol tracking loop filters
- High performance Maximum Likelihood (ML) timing error detector
- Preamble detection
- Lock detector
- Symbol decision
- Bit-true, cycle-true MATLAB model

### APPLICATIONS

- Satellite receivers
- Communications testing equipment
- Security and surveillance equipment

### HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

### DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5 family
- User manual and implementation guide
- Application engineering support hotline/email



### DESCRIPTION

The IP-PSK-DEMOD core provides demodulation for Phase Shift Keyed (PSK) data in a compact FPGA IP core. The demodulation mode is dynamically programmable for M=2, 4, or 8 phase demodulation. This core also includes AGC, matched filtering, carrier recovery, timing recovery, symbol decision, and preamble detector logic providing a complete PSK demodulation solution for the communication systems.

The PSK demodulator core processes 16 bit baseband In-Phase (I) and Quadrature (Q) data. The input data rate is required to be 8 times of the symbol rate. The main data path includes a matched filter using Root Raised Cosine filter (RRC), AGC, resampler using Fractional Delay (FD) filter, and a complex multiplier. The coefficient reloadable RRC filter is used as matched filter to eliminate inter-symbol interference (ISI). Following the RRC filter the AGC is used to maximize the dynamic range of the signal magnitude and maintain an optimal output sample level for symbol decision. Outputs of the AGC is resampled by the FD filter at symbol clock, which is built by the timing recovery loop. In the timing loop error detector Maximum Likelihood based spectrum analysis technique is provided to achieve an asymptotically jitter free timing error estimate. The resampled I/Q data is multiplied by the NCO outputs to remove any residual carrier frequency. Finally the symbol decision component encodes the demodulated I/Q samples into 8-bit hard-coded symbols according to user input mapping table. Both demodulated I/Q samples and hard-coded symbols are available at the outputs. The lock detector monitors the timing and carrier loop errors and asserts a lock signal when both accumulated errors are within the threshold during a predefined amount of time.

The core is targeted at the Xilinx Virtex-5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex-5 designs with the constraints and implementation control files provided.

MATLAB/Simulink simulation models for system design are provided with test vectors. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

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01/26/11

# IP-PSK-DEMODO

## Ordering Information

Product	Part Number	Description
IP-PSK-DEMODO	58001-0	Netlist version bundled with X6/X5 boards
	58001-1	Netlist Version Only
	58001-2	Source Code Version

Table 1. Product information

## Block Diagram

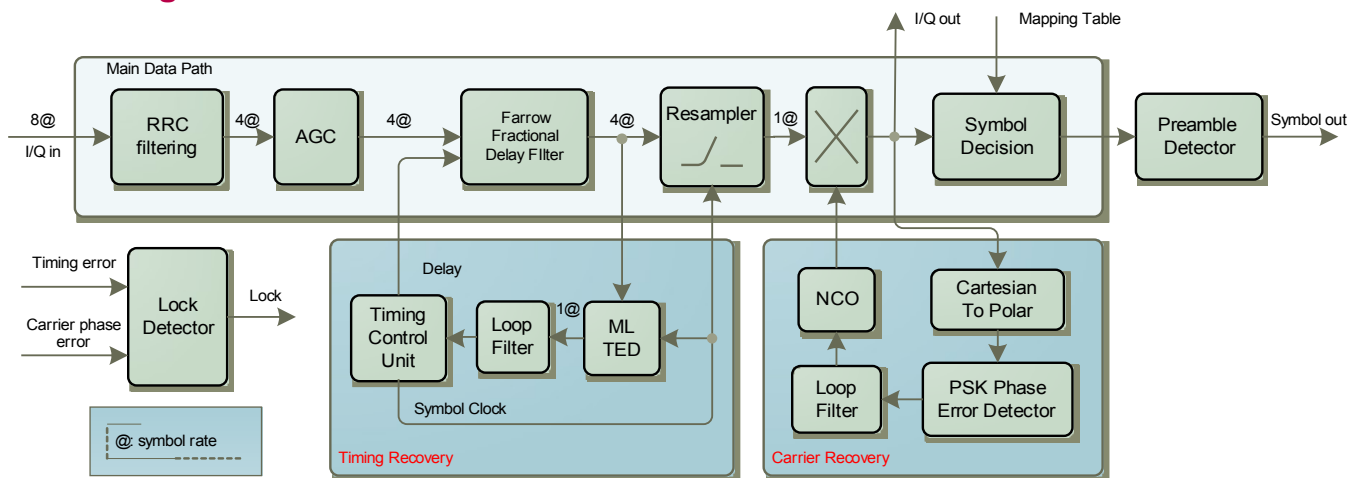


Figure 1. PSK demodulator block diagram

The RRC filter is placed as the match filter to eliminate ISI. A high performance Maximum Likelihood timing error detector (TED) is implemented to generate jitter free timing error and considered to be an optimal approach for the current digital demodulator design. Farrow structure FD filter, serving as an interpolation filter, provides intermediate data between adjacent samples for the highest SNR output. Carrier recovery loop takes one sample per symbol, detects the phase error, feeds back the error information to the sine/cosine table (or NCO) through a second order loop filter, and remove the residual carrier frequency.

As shown in Figure 1, limited by the timing error range of the timing recovery loop, the core requires the input data rate to be eight times of the symbol rate. The core can get the most information while operating in the timing error range.

# IP-PSK-DEMOD

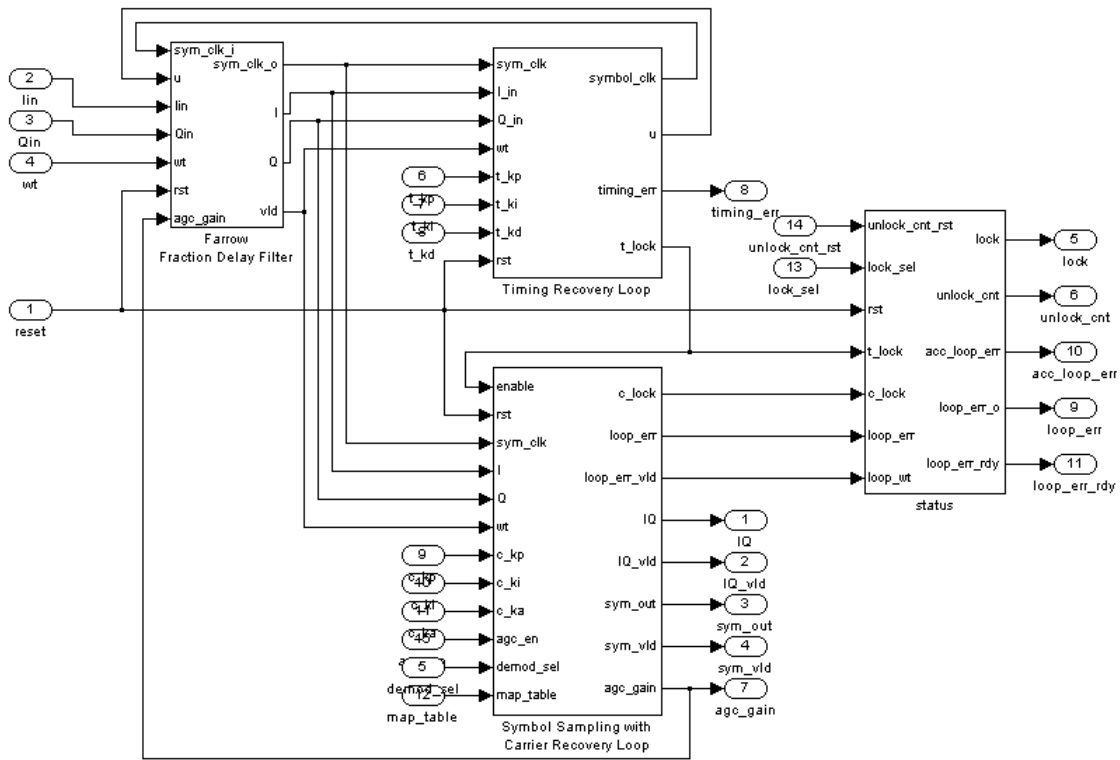


Figure 2. MATLAB/Simulink project of PSK demodulator

Figure 2 shows the PSK demodulator built under MATLAB/Simulink environment using Xilinx System Generator blockset. All the signal processing blocks utilize cores from Xilinx System Generator and guaranteed to be bit true and cycle true as in the FPGA hardware. In Figure 3, the core is integrated with the analog front end, a multichannel DDC, and II FrameWork logic components for the Software Defined Radio (SDR) project on X5-210M. This system is built on the COTS (Commercial Off-The-Shelf) product, providing high performance and full upgrades to the next generation hardware using the same IP core.

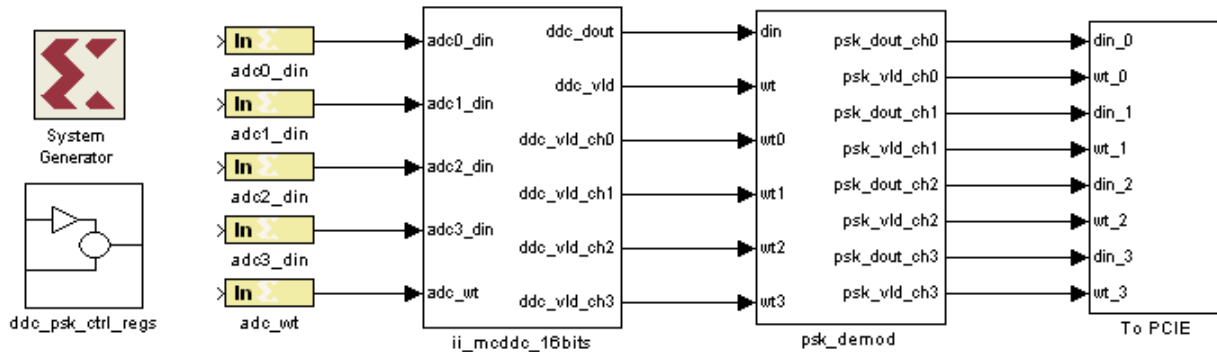


Figure 3. MATLAB/Simulink system integration of DDC and PSK demodulator

# IP-PSK-DEMOD

## Bit Error Rate (BER) Performance

The BER performance of the PSK demodulation core versus  $E_b/N_0$  is shown below. The data is measured by the imbedded preamble detector (PD), which looks for the preamble in the signal, compares with the given preamble information, and calculate the BER. Solid and dashed curves are theoretical BER values, and markers are BER measurements under different noisy environment. BER of BPSK signal is right on the theoretical curve; BER of QPSK and 8PSK signal are within 1 dB from the curve. The BER will be improved after Forward Error Correction (FEC).

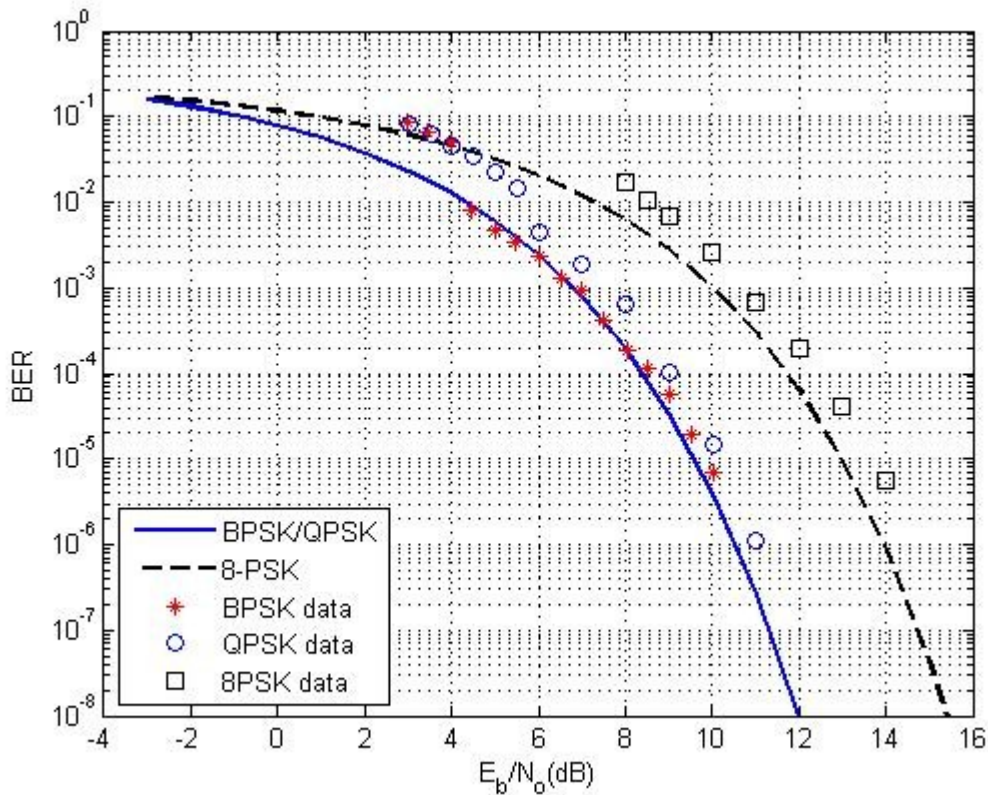


Figure 4. BER versus  $E_b/N_0$ . The solid and dash lines are theoretic curve from [Wikipedia](#).

# IP-PSK-DEMOD

## Port Descriptions

Signal	Size	Direction	Description
clk_1	1	In	Clock; 200 MHz or faster.
ce_1	1	In	Clock enable; set to '1'.
psk_ch_num	8	In	PSK channel number for multi-channel configuration
psk_reset	1	In	Asynchronous reset for PSK core, active high
psk_reset_wt	1	In	Write strobe of psk_reset
iq_din	16	In	Interleaved real/imaginary data input
iq_wt	1	In	Write strobe of input I/Q data
demod_sel	3	In	Demodulation type selection
demod_sel_wt	1	In	Write strobe of demod_sel
rrc_coef	16	In	RRC filter coefficient input
rrc_coef_wt	1	In	Write strobe of rrc_coef
agc_en	1	In	AGC enable
agc_en_wt	1	In	Write strobe of agc_en
map_table	24	In	Mapping table for symbol decision
map_table_wt	1	In	Write strobe of map_table
iq_dout	8	Out	Demodulated I/Q data; bit 15..8 => I; bit 7..0 => Q
iq_vld	1	Out	Valid strobe of iq_dout
sym	8	Out	Hard coded symbol output
sym_vld	1	Out	Valid strobe of sym
psk_err	8	Out	PSK carrier loop error
psk_err_rdy	1	Out	Ready signal of psk_err
lock	1	Out	PSK lock signal
pd_rst	1	In	Preamble detector reset
derotate_en	1	In	Enable symbol derotation according to the given preamble information
bs_err_cnt_sel	1	In	Select bit/symbol error
preamble	27	In	Preamble information
frame_size	16	Out	Frame size between two preambles
preamble_cnt	16	Out	Preamble counter output
bs_err_cnt	16	Out	Bit/symbol error counter output

**Table 2. I/O port table**



# IP-PSK-DEMOD

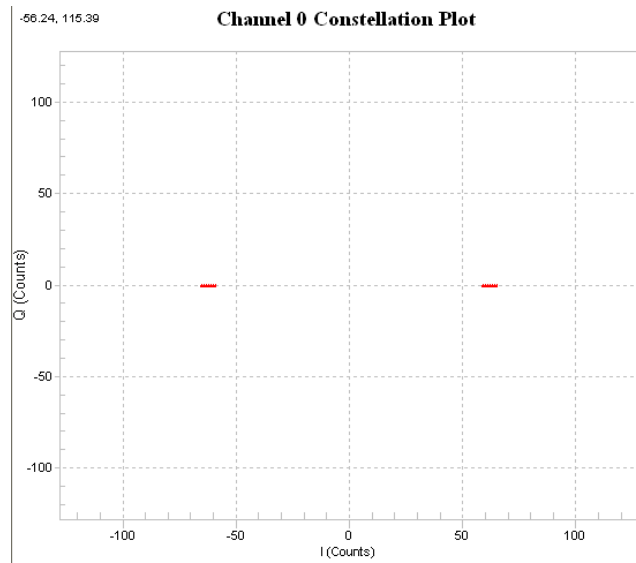


Figure 8. Demodulated BPSK constellation without noise

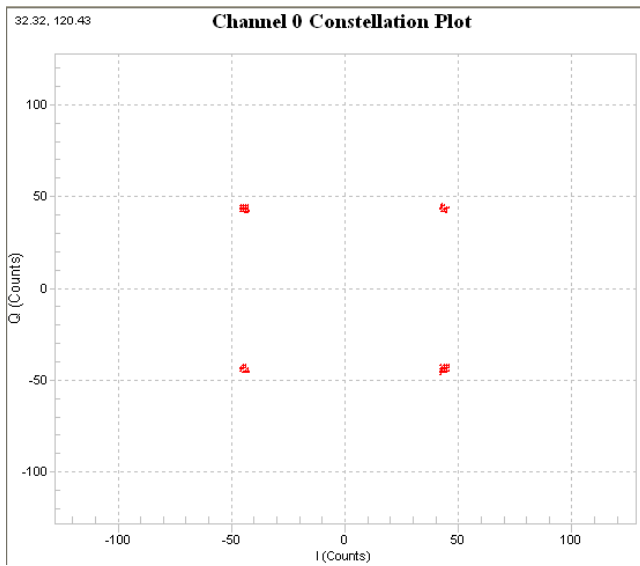


Figure 9. Demodulated QPSK constellation without noise

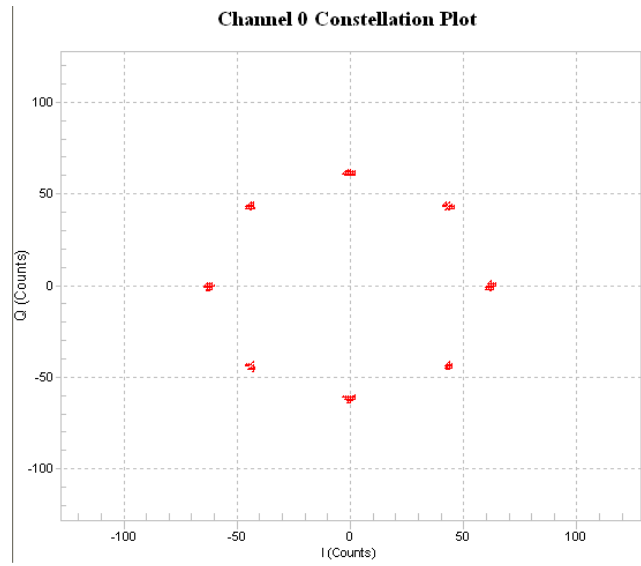


Figure 10. Demodulated 8-PSK constellation without noise

# IP-PSK-DEMOD

## Standard Features

Inputs			
Input Channel Number	1		
Input Format	16-bit, 2's complement, complex interleaved		
Input Rate	<b>Symbol rate x8</b>		
Outputs			
Output Channel Number	1		
Output Format	Demodulated I/Q: 8-bit, 2's complement Symbol: 8-bit, unsigned		
Demodulation			
Type	BPSK, QPSK, 8-PSK		
Symbol Rate	Up to 1.4 MSPS		
Timing Error Range	+- 1% of symbol rate		
Frequency Error Range	+- 5% of symbol rate		
Acquisition Time	< 850 ms (QPSK at Eb/No = 5.5 dB, symbol rate = 10 KSPS)		
	BPSK	QPSK	8-PSK
Minimum Eb/No	5.5 dB	6 dB	11 dB
Root Raised Cosine Filter	Programmable in ini file		
Power Consumption	0.206 Watt		

Note: The core requires 200 MHz or faster clock.

Device Utilization		
1 Channel		
Element	FPGA Resource	Virtex-5 SX95T
LUT	6785	11.5%
FF	9099	15.5%
DSP48E	138	21.6%
BlockRAM	22	9%

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Mailing Address: Innovative Integration, Inc.

2390A Ward Avenue, Simi Valley, California 93065

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