

IP-RI-CHTU128/256



v1.0

128 OR 256 Channel Digital Downconversion Core for FPGA

FEATURES

- 128 or 256 individually tuned DDC channels
- Real or complex 16-bit, 210 MHz inputs
- Tuning resolution $F_s/2^{32}$
- Filter rejection >80 dB
- Decimation rates from $F_s/512$ to $F_s/16383$
- Fractional resampler with 30 bit resolution
- Gain from 0 to 60 dB in 0.07 dB steps
- Supports Xilinx Virtex5 FPGA

APPLICATIONS

- Base stations
- Image Processing
- Surveillance

IMPLEMENTATION SUPPORT

- Fixed and floating point simulation models in C and MATLAB
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

HARDWARE SUPPORT

- Innovative X5-400M XMC Module

DESCRIPTION

The IP-RI-CHTU128/256 core has up to 256 individually tunable channels of digital down-conversion (DDC) with filtering. This patented core from R-Interface provides a uniquely flexible front-end to multi-channel receivers, providing high channel density with frequency translation, decimation and channel filtering for baseband signal recovery as FPGA firmware.

Each channel has programmable tuning, gain control and decimation rate, with flexible output data rates using a fractional resampler. The input is 16-bit real or complex data at sample rates (F_s) to 210 MHz. The dynamic range of the core exceeds 90 dB for 16-bit inputs, with an 80 dB channel-to-channel rejection. DDC tuning resolution is 6 mHz, with an alias-free baseband as wide as $0.8 F_s/512$.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and is available in either 128 or 256 channel version. The 32-channel core consumes about 60% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

The IP-RI-CHTU128/256 core has been ported to Innovative's X5-400M XMC IO module and may be purchased as part of a pre-configured X5-400M. No logic design is required for this version. This high performance, PCI Express XMC module features two 14-bit, 400MSPS inputs, a Virtex5 SX95T device, and 512MB of memory. Software drivers provide controls and data flow support for Windows and Linux applications.

Simulation models for system design are provided as fixed point or floating point C and MATLAB. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.

This core was developed by and is licensed through R-Interface. Innovative Integration provides application and technical support for this core. Core updates and customization is provided by R-Interface.



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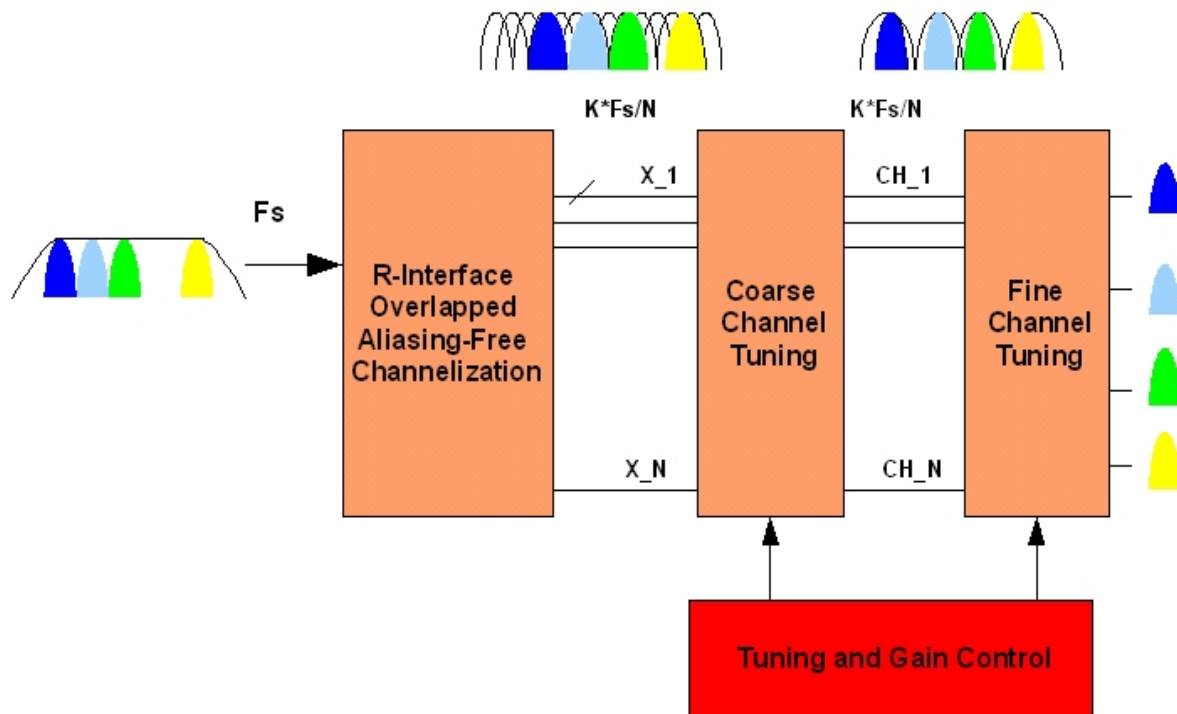
IP-RI-CHTU128/256

ORDERING INFORMATION

Product	Part Number	Description
IP-RI-CHTU128/256	58006	IP core for 128 or 256 independent DDC channels, netlist version, Virtex SX95T target
X5-400M XMC module with 128 or 256 DDC channels	80180-7	X5-400M PCIe/XMCe Module w/SX95T FPGA, D/A clk: PLL (interpolating), IP-RI-CHTU128/256 logic core installed, BIT file only

Block diagram

The R-Interface tunable parallel channelizer is shown below. The first stage performs an overlapped aliasing-free channelization, the second stage implements a cross bar switching matrix allowing to choose N selected channels among 2N overlapped channels. In the last stage, the system performs fine tuning and filtering over the selected channels. The two last stages are control by user-defined tuning parameters. The tuning parameters are the set of filter coefficients as well as the set of channel central frequencies.



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Port Descriptions

Signal	Size	IO	Description
SYST_CLK	1	I	System clock for the design. All the design operates on rising edge of SYST_CLK.
RESET	1	I	IP asynchronous reset. Reset active level is high (RESET=1).
VALID_IN	1	I	Sample clock in. Input data are synchronous on this clock.
SPL_CLK_IN	1	I	M bits in quadrature part of the complex input.
DIN_Q[M-1:0]	M	I	M bits in phase part of the complex input.
DIN_I[M-1:0]	M	I	Address bus size factory defined
M_ADD [AB-1:0]	7	I	Microprocessor access input data bus.
M_DATA_IN[DB-1:0]	32	I	Microprocessor access output data bus.
M_DATA_OUT[DB-1:0]	32	O	Chip select .
IP_SEL	1	I	Write access - Level is factory defined
M_WRITE	1	I	Read access - Level is factory defined
M_READ	N	I	N bits in quadrature part of the complex output
DOUT_Q[P-1:0]	N	O	N bits in phase part of the complex output
DOUT_I[P-1:0]	1	O	Sample clock out. Output data are synchronous on this clock rising edge.
SPL_CLK_OUT	1	O	Data out valid. Active high
VALID_OUT	1	O	Valid output signal for channel i complex output components. Active high.

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Standard Features

Inputs	
Inputs	1
Input Format	16-bit, 2's complement, real or complex
Sample Rate	210 MHz maximum (-4 device speed grade)
Outputs	
Outputs	128 or 256
Output Type	Complex I & Q
Output Format	16-bit, 2's complement
Output Rate	Fs/512 to Fs/16384
Channel Tuning	
Tuning Range	-Fs/2 to +Fs/2
Tuning Resolution	Fs/2 ³²
Max Alias-Free Bandwidth	0.8*Fs/512 (128 channel) 0.8*Fs/1024 (256 channel)
Gain	
Range	0 to 60 dB
Resolution	0.07 dB
Channel Filter	
Rejection to adjacent channel	80 dB

Performance	
SFDR	>90 dB
S/N	>85 dB

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
SLICES	128 channel = 8.5K 256 channel = 9K	58% 62%
BlockRAM	128 channel = 150 256 channel = 160	30.5% 32.8%

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