

IP-RI-FR21

Fractional Resampler Core

FEATURES

- Fractional resampler for 1 to 0.5 ratios
- 2^{30} resampling ratio resolution
- Real or complex 16-bit, 250 MHz inputs
- SFDR > 90dB
- Supports Xilinx Virtex5 FPGA

APPLICATIONS

- Wireless receivers
- Image Processing
- Audio Processing

IMPLEMENTATION SUPPORT

- Fixed and floating point simulation models in C and MATLAB
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

DESCRIPTION

The IP-RI-FR21 core provides extremely precise sample rate conversion over a range of 0.5 to 1 with 30 bits resolution. The fractional resampler core can sample a complex input signal D_{in} , sampled at FS_{in} , into a complex output signal, D_{out} , sampled at FS_{out} . FS_{out} can be programmed, with an extremely high precision, to values covering the range $[FS_{in}; FS_{in}/2]$. FS_{out} can also be dynamically corrected regarding external clock frequency error command. The FR21 IP has been designed in order to best adapt its complexity to the ratio between FS_{in} and the system clock (FS_{sys}) via a set of synthesis level generic parameters.

The IP can work as a stand alone function or can be easily integrated into a complete design. FR21 is configured via a user defined processor interface, allowing the system to take control of all the features.

The core is targeted at the Xilinx Virtex5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

Simulation models for system design are provided as fixed point or floating point C and MATLAB. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.



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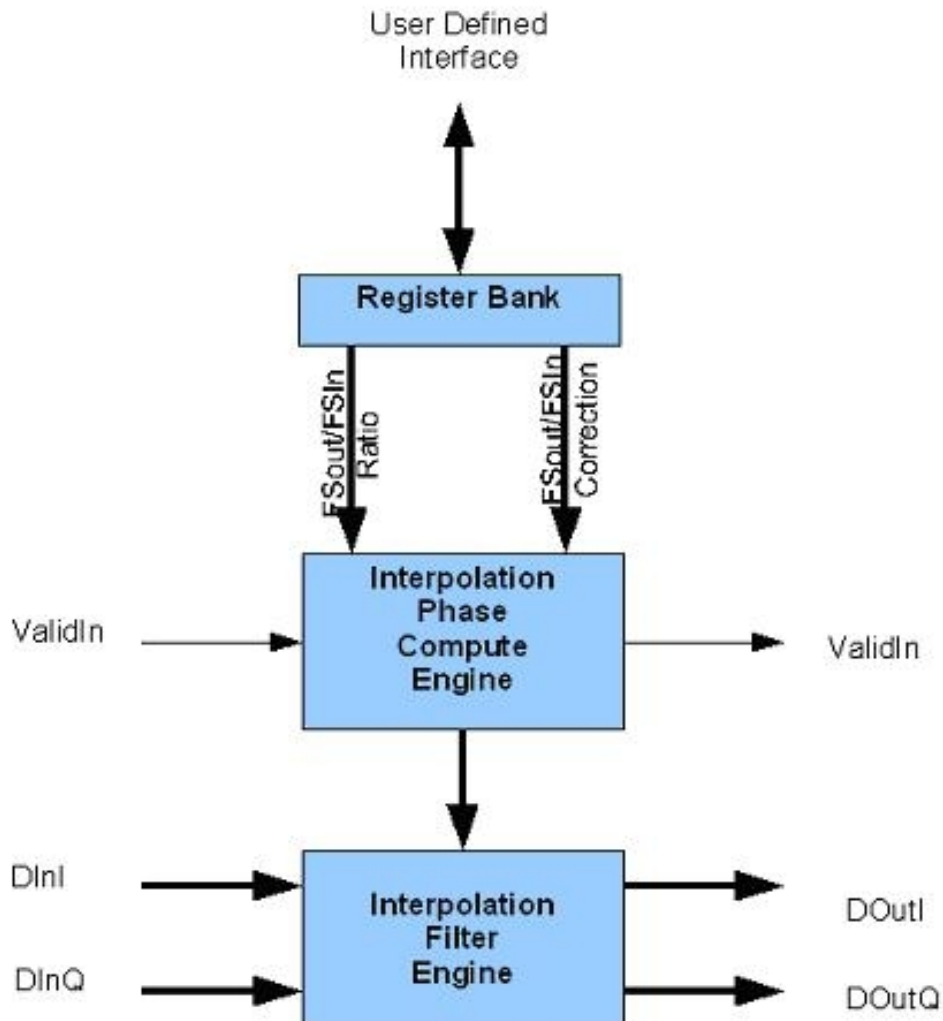
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ORDERING INFORMATION

Product	Part Number	Description
IP-RI-FR21	58008	IP core fractional resampler, netlist version, Virtex SX95T target

Block diagram



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Port Descriptions

Signal	Size	IO	Description
Fsin	1	I	Input clock.
Fsout	1	I	Output clock.
RESET	1	I	IP asynchronous reset. Reset active level is high (RESET=1).
VALID_IN	1	I	Sample clock in. Input data are synchronous on this clock.
DIN_Q[M-1:0]	M	I	M bits in phase part of the complex input.
DIN_I[M-1:0]	M	I	Address bus size factory defined
DOUT_Q[P-1:0]	N	O	N bits in phase part of the complex output
DOUT_I[P-1:0]	1	O	Sample clock out. Output data are synchronous on this clock rising edge.
VALID_OUT	1	O	Valid output signal for channel i complex output components. Active high.

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Standard Features

Inputs	
Inputs	1
Input Format	16-bit, 2's complement, real or complex
Sample Rate	250 MHz maximum (-4 device speed grade)
Outputs	
Outputs	1
Output Type	Complex I & Q
Output Format	16-bit, 2's complement
Output Rate	
Resampling Rates	
Ratio Range	+/- 30.5 ppm to +/-61 ppm
Resolution	$9.31 \cdot 10^{-3}$ to $1.86 \cdot 10^{-2}$ ppm
Frequency Response	
Bandwidth (Alias Free)	$F_{sin}/8$
Passband Attenuation	<0.05 dB, BW = $F_{sin}/4$ <0.7 dB, BW = $F_{sin}/2$

Performance	
S/N	>80 dB

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
DSP48E	1:2 range : 9	1.5%
	2:4 range : 5	0.8%
	4:8 range : 3	0.5%
	>8 range : 2	0.3%
BlockRAM	1:2 range : 2	0.5%
	>2 range : 1	0.16%

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