

IP-RI-DDC16/32



v1.0

16 OR 32 Independent Channel Digital Downconversion Core for FPGA

FEATURES

- 16 or 32 independent DDC channels
- Up to 8 input, 16-bit @ 210 MSPS
- Tuning resolution $F_s/2^{37}$
- SFDR > 90 dB
- Decimation rates from 128 to 65536
- Programmable 121 tap pulse shaping filter
- Up to 60 dB gain, 0.07 dB resolution
- Supports Xilinx Virtex5 FPGA

APPLICATIONS

- Digital Receivers
- Image Processing
- Spectral Analysis

IMPLEMENTATION SUPPORT

- Fixed and floating point simulation models in C and MATLAB
- Testbench with test vectors
- Implementation control files
- User manual and implementation guide
- Application engineering support hotline/email

HARDWARE SUPPORT

- Innovative X5-400M XMC Module

DESCRIPTION

The IP-RI-DDC16/32 core has up to 32 independent output channels of digital down-conversion (DDC). As a flexible front-end to receivers and imaging devices, this core implements the frequency translation for baseband signal recovery as FPGA firmware.

Each channel has programmable tuning, filtering, gain control and decimation rate. Up to 8 16-bit inputs are supported at sample rates (F_s) to 210 MHz. The dynamic range of the core exceeds 90 dB for 16-bit inputs. DDC tuning accuracy is 1 mHz, with an alias-free baseband as wide as $F_s/256$.

The core is targeted at the Xilinx Virtex5 SX95T FPGA and is available in either 32 or 16 channel version. The 32-channel core consumes about 60% of an SX95T device. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASICs.

The IP-RI-DDC16/32 core has been ported to Innovative's X5-400M XMC IO module and may be purchased as part of a pre-configured X5-400M. No logic design is required for this version. This high performance, PCI Express XMC module features two 14-bit, 400MSPS inputs, a Virtex5 SX95T device, and 512MB of memory. Software drivers provide controls and data flow support for Windows and Linux application.

Simulation models for system design are provided as fixed point or floating point C and MATLAB. The testbench is bit-true, cycle-true for device simulation. Source is available for purchase.

This core was developed by and is licensed through R-Interface. Innovative Integration provides application and technical support for this core. Core updates and customization is provided by R-Interface.



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09/10/08

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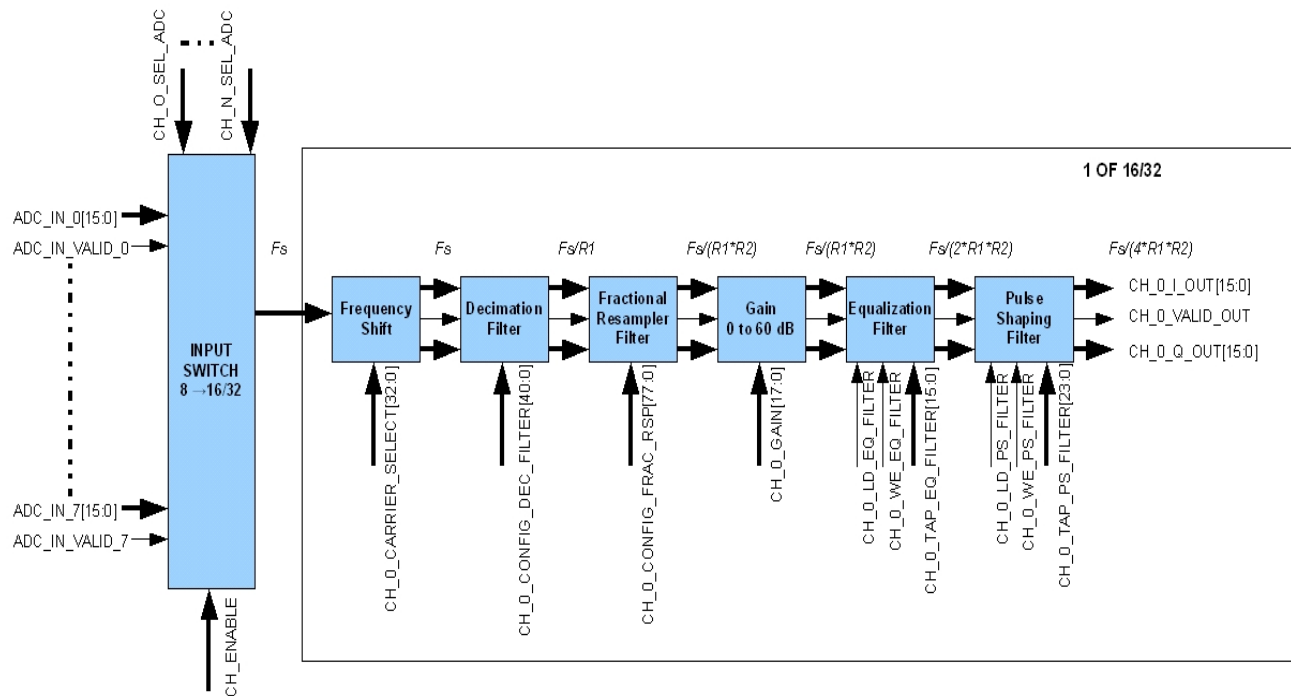
IP-RI-DDC16/32

ORDERING INFORMATION

Product	Part Number	Description
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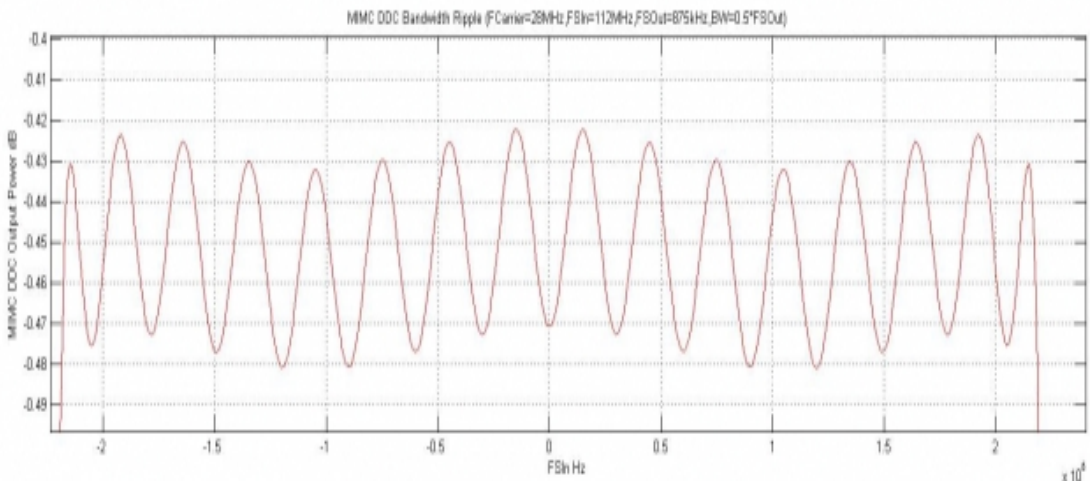
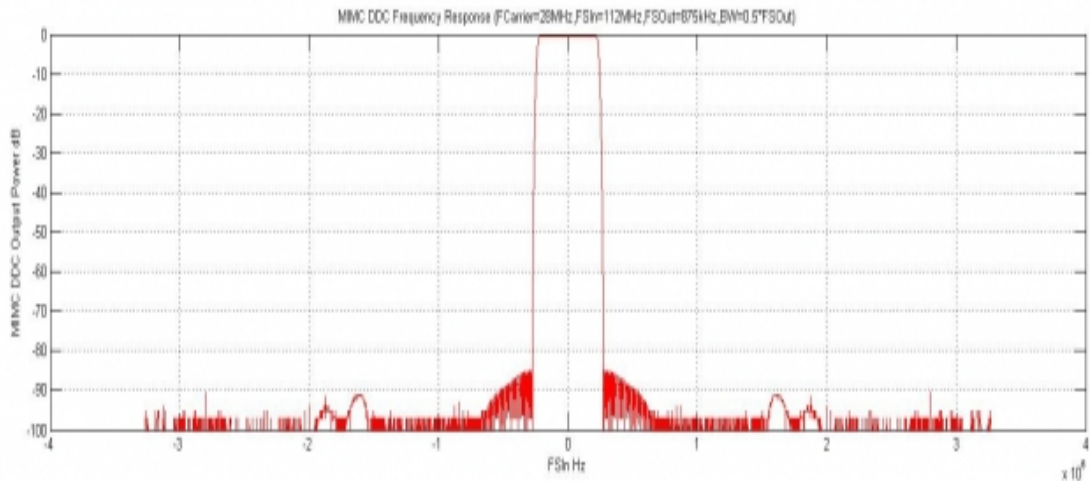
IP-RI-DDC16/32

IP-RI-MDDC16	58004	IP core for 16 independent DDC channels, netlist version, Virtex SX95T target
IP-RI-MDDC32	58005	IP core for 32 independent DDC channels, netlist version, Virtex SX95T target
X5-400M XMC module with 16 DDC channels	80180-5	X5-400M PCIe/XMCe Module w/SX95T FPGA, D/A clk: PLL (interpolating), IP-RI-MDDC16 logic core installed, BIT file only
X5-400M XMC module with 32 DDC channels	80180-6	X5-400M PCIe/XMCe Module w/SX95T FPGA, D/A clk: PLL (interpolating), IP-RI-MDDC32 logic core installed, BIT file only



IP-RI-DDC16/32

Port Descriptions



Signal	Size	IO	Description
SYST_CLK	1	I	System clock for the design. All the design operates on rising edge of SYST_CLK.
HARD_RESET	1	I	IP asynchronous reset. Reset active level is high (HARD_RESET=1).
SCLR	1	I	IP synchronous reset. Reset active level is high (SCLR=1).
ADC_IN_k	16	I	Real input k of the IP (k ranging from 0 to NB_IN-1). Signed 16 bits 2's complement format. Sampled by the IP when ADC_IN_VALID_k=1.
ADC_IN_VALID_k	1	I	Valid signal for input ADC_IN_k. Active level high.
CH_ENABLE	NB_CH	I	Enable the MIMC DDC channels. When CH_ENABLE(i)=1, channel i is enabled

IP-RI-DDC16/32

			otherwise it is disabled.
CH_i_SEL_ADC	NB_IN	I	Enable DDC channel i to select one of the NB_IN input. The index of the first LSB equal to 1 gives the index of the selected input.
CH_i_CARRIER_SELECT	33	I	Programming bus for the Frequency Shift unit of channel i. Computed and formatted by the IP Driver.
CH_i_CONF_DEC_FILTER	41	I	Programming bus for the Dec Filter unit of channel i. Computed and formatted by the IP Driver.
CH_i_CONF_FRAC_RSP	77	I	Programming bus for the Fractional Resampler unit of channel i. Computed and formatted by the IP Driver.
CH_i_GAIN	17	I	Programming bus for the Gain unit of channel i. Computed and formatted by the IP Driver.
CH_i_LD_EQ_FILTER	1	I	Signal used to initiate an Equalization Filter tap programming. Active high.
CH_i_WE_EQ_FILTER	1	I	Equalization Filter tap write enable signal. Active high.
CH_i_TAP_EQ_FILTER	16	I	Equalization Filter taps. Signed 16 bit, 2's complement format. Computed and formatted by the IP Driver.
CH_i_LD_PS_FILTER	1	I	Signal used to initiate an Equalization Filter tap programming. Active high.
CH_i_WE_PS_FILTER	1	I	Pulse Filter tap write enable signal. Active high.
CH_i_TAP_PS_FILTER	24	I	Pulse Shaping Filter taps. Signed 24 bit, 2's complement format. Computed and formatted by the IP Driver.
CH_i_I_OUT	16	O	Channel i in phase complex output component. Signed 16 bit, 2's complement.
CH_i_Q_OUT	16	O	Channel i in quadrature complex output component. Signed 16 bit, 2's complement.
CH_i_VALID_OUT	1	O	Valid output signal for channel i complex output components. Active high.

IP-RI-DDC16/32

Standard Features

Inputs	
Inputs	8
Input Format	16-bit, 2's complement, real
Sample Rate	210 MHz maximum (-4 device speed grade)
Outputs	
Outputs	16 (IP-RI-MDDC16 Core) 32 (IP-RI-MDDC32 Core)
Output Type	Complex I & Q
Output Format	16-bit, 2's complement
Output Rate	Fs/128 to Fs/65536
Channel Tuning	
Tuning Range	-Fs/2 to +Fs/2
Tuning Resolution	Fs/2 ³⁷
Max Alias-Free Bandwidth	Fs/256
Gain	
Range	0 to 60 dB
Resolution	0.07 dB
Pulse Filters	
Taps	121
Tap Resolution	24-bit

Performance	
SFDR	>90 dB
S/N	>85 dB

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
DSP48E	384	59.6%
LUT	31K	52.6%
FF	32K	54.4%
BlockRAM	112	50%

IP-RI-DDC16/32

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Mailing Address: Innovative Integration, Inc.

2390A Ward Avenue, Simi Valley, California 93065

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