IP-XLFFT

v1.1

IP Core for 64K to 1M Point FFT with Windowing Functions

FEATURES

- Logic core for 64K to 1M points FFT
- Transform size reconfigurable
- Runtime modes: 1-D FFT, 2-D FFT
- Forward or inverse mode
- 13% of Xilinx Virtex5 SX95
- FPGA clock rates up to 300 MHz
- 16-bit complex inputs, 24-bit complex outputs
- Natural order outputs
- Bit-true, cycle-true MATLAB model

APPLICATIONS

- Spectrum analyzers
- Signal Intelligence
- Image processing

HARDWARE SUPPORT

- Support Xilinx Virtex-6, Virtex-5 FPGA
- Innovative X5 and X6 family of XMC Modules

DELIVERABLES

- Netlist or MATLAB/Simulink source code
- MATLAB/Simulink simulation model with test vectors
- Implementation control files for Innovative X5/X6 family
- User manual and application notes

Description

The IP-XLFFT logic core includes a pipelined FFT computation engine, a CORDIC Rotator for twiddle factor computation, and a QDR SRAM memory controller with address generation. The processed spectrum data is available for unloading from the QDR SRAM in natural order.

The pipelined FFT computation engine allows continuous data processing and maximizes the core computation and data transfer efficiency. Intermediate data are stored in the on chip Block Ram or the off chip QDR SRAM. In this design only one memory bank is required for intermediate data buffer. Twiddle factors are computed using a CORDIC Rotator that consumes only adders for calculation, resulting in compact logic usage.

The core is targeted at the Xilinx Virtex5 SX95T FPGA. The IP core is provided as a netlist and may be rapidly integrated into Virtex5 designs with the constraints and implementation control files provided. Support is available for targeting other FPGA devices or ASIC.

Simulation models for system design are provided as fixed point MATLAB/Simulink files. The model is bit-true, cycle-true for device simulation. Source is available for purchase.

04/04/11

IP-XLFFT

Ordering Information

Product	Part Number	Description
IP-XLFFT	58011-0	Netlist version bundled with X6/X5 boards
	58011-1	Netlist Version Only
	58011-2	Source Code Version

Table 1. Product information

Block diagram

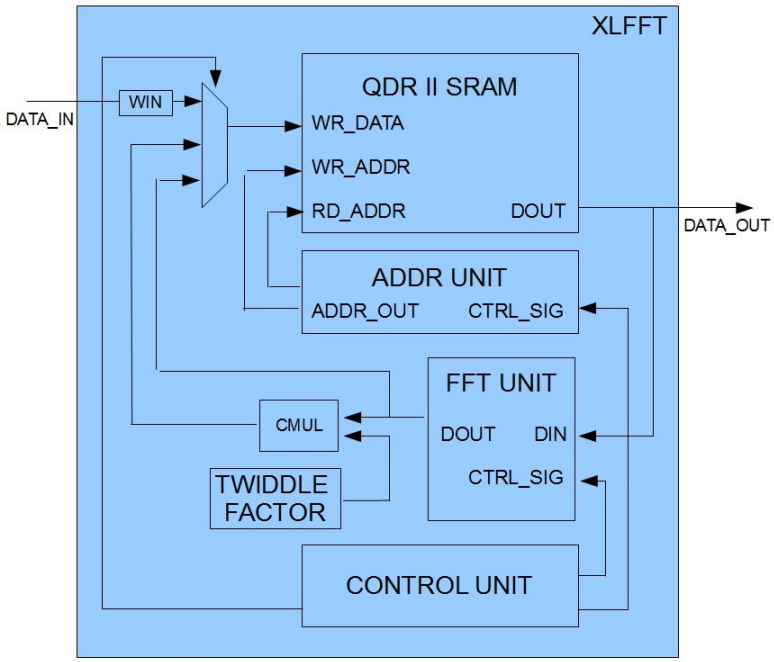

Figure 1. IP-DDC block diagram

Windowing Functions

The IP-Windowing core provides these data windowing functions frequently used in IP-XLFFT core.

Window	Best for signal types	Frequency Resolution	Spectral Leakage	Amplitude Accuracy
Blackman	Random or mixed	Poor	Best	Good
Boxcar (uniform)	Random	Best	Poor	Poor
Hann	Random	Good	Good	Fair

Table 2. Available windowing functions

IP-XLFFT

Performance

Size	Size Configurable	Output Bits	Max Frame Rate(KHz)	Overlap up to (%)	Engine	FF(%)	LUT(%)	On Chip BRAM (%)	DSP48E (%)	External Memory Usage	Memory Type	Architecture
1K	No	18	1342.77	63.64	5	34.24	28.76	12.5	50	0	On-chip	pipelined
2K	No	18	537.11	54.55	4	31.39	26.05	18.33	47.5	0	On-chip	pipelined
4K	No	18	268.55	54.55	4	33.93	28.22	23.35	43.8	0	On-chip	pipelined
8K	No	24	100.71	39.39	3	33.57	27.5	36.26	42.23	0	On-chip	pipelined
16K	No	24	33.57	9.09	2	24.05	19.92	45.84	29.4	0	On-chip	pipelined
16K	Yes	24	2.51	0	1	13.9	12.9	2.5	11.25	128KB	External	pipelined
32K	No	24	8.39	0	1	13.01	11.05	43.75	16.58	0	On-chip	pipelined
64K	No	24	1.05	0	1	6.22	4.79	52.92	6.26	0	On-chip	Radix-4
64K	Yes	24	0.64	0	1	13.9	12.9	2.5	11.25	512KB	External	pipelined
256K	Yes	24	0.16	0	1	13.9	12.9	2.5	11.25	2MB	External	pipelined
1M	Yes	24	0.04	0	1	13.9	12.9	2.5	11.25	8MB	External	pipelined

Notes: 1. External memory refers to QDRII SRAM @ 166MHz; 250MHz operation results in ~25% improvement; 2. FGPA system clock @ 275MHz. 3. Input data rate is 500MSPS.

Table 3. II_XLFFT performance specifications with a X5-G12 Virtex5 XC5VSX95T-2FF1136C device

Port Description

Signal	Size	Direction	Description
reset	1	In	Asynchronous reset, active high.
clk	1	In	clock
ce	1	In	Clock enable
din_I	16	In	Data in
din_Q	16	In	Data in
din_we	1	In	Data in write strobe.
NFFT	5	In	log2 (point size)/2
FFT_scale_sch	10	In	Scaling schedule
FFT_fwd_inv	1	In	Forward FFT (FFT_fwd_inv=1) or inverse FFT (FFT_fwd_inv=0)
D	1	In	1D FFT (D=0) or 2D FFT (D=1)
start	1	In	FFT start
win_sel	2	In	Window function selection, '00'-Boxcar, '01'-Hann, '10'-Blackman
qdr_w_rdy	1	In	QDRII SRAM write ready
qdr_rdata_rdy	1	In	QDR II SRAM data read ready
qdr_raddr_rdy	1	In	QDR II SRAM address read ready
qdr_dout	64	In	QDR II SRAM data out
dither_en	1	In	Phase dither on
qdr_wren	1	Out	QDR II SRAM data/address write strobe
qdr_waddr	20	Out	QDR II SRAM address write
qdr_wdata	64	Out	QDR II SRAM data write
qdr_rden	1	Out	QDR II SRAM data read enable
qdr_raddr_wr	1	Out	QDR II SRAM address read strobe
qdr_raddr	20	Out	QDR II SRAM address read
Frame_size	10	Out	sqrt(point size)
FFT_OVFLO	1	Out	FFT overflow indicator (Active high)
FFT_DONE	1	Out	FFT done strobe (Active high)

Table 4. I/O port table

IP-XLFFT

Standard Features

Inputs	
Inputs	Complex (I/Q)
Input Format	16-bit, 2's complement
Outputs	
Outputs	Complex (I/Q)
Output Format	24-bit, 2's complement
FFT	
Output Formats	Natural order
Transforms	1-D or 2-D FFT, IFFT
Window Functions	Hann, Blackman, Uniform

Device Utilization		
Element	FPGA Resource	Virtex5 SX95T
FF	7584	12.9%
LUT	8162	13.9%
DSP48E	72	11%
BlockRAM	6	2%

IP-XLFFT

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