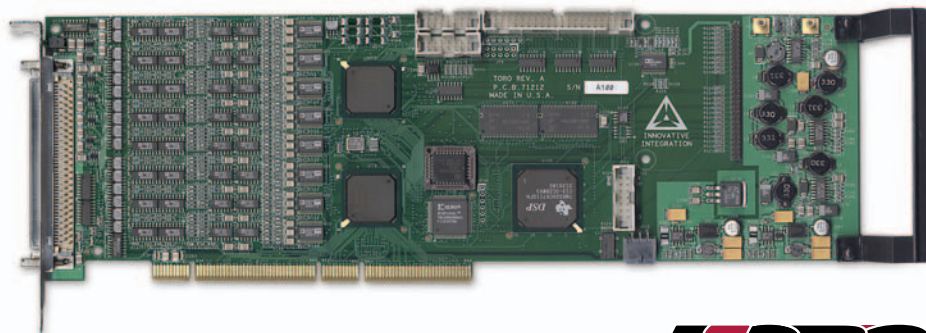


Toro

16 Simultaneous A/D to 250 KSPS
900MFLOPS Floating Point
TMS320C6711 DSP



Features

150MHz TMS320C6711 DSP (floating point)
16 Independent Analog I/O Channels to 250kHz
Flexible trigger mode: pre/post threshold
32 or 64 bit PCI
Real Time Event Log
Multiboard Synchronization (CikLink, SyncLink)
64 Bits Digital I/O

Applications

High Channel Vibro/Acoustic Monitoring
High Channel Servo Controller
State Space Control
Optical Switch Control
Complex Data Acquisition Schemes

Hardware Options

FIFOCable
100 Pin MDR Breakout
CodeHammer Debugger

Software Development Tools

Pismo Toolset
Armada Toolset
TI Code Composer Studio

Ordering Information

Toro-16	80059-0
Toro-8	80059-1
Toro-16 DevPack	90059-0
Toro-8 DevPack	90059-1

DevPack Available



Please visit us at
www.innovative-dsp.com/devpack
for details

Overview

The Toro card is perfect for servo control and data acquisition applications requiring high performance DSP with precision 16-bit analog. Its high-performance 32-bit floating-point DSP controls up to 16 simultaneous channels of independent A/D and D/A conversion with flexible trigger modes. The Toro's high performance 32/64 bit PCI interface is capable of up to 264 Mbytes/sec data bursts, which makes it ideal for data-intensive applications. The Toro board shares many features with other boards in the Matador product line. These features are presented in more details in the overview section of the Matador Series.

Processing Core

Toro employs a TMS320C6711 32 bit floating point DSP as the data movement/processing engine. On-chip resources include two 32 bit counter/timers, sixteen DMA channels, 64 Kbytes of dual-access SRAM and a prioritized interrupt controller. Memory on Toro includes 32 Mbytes of 1 wait-state synchronous DRAM (SDRAM) which utilizes an on-chip L1/L2 cache controller to achieve near on-chip performance.

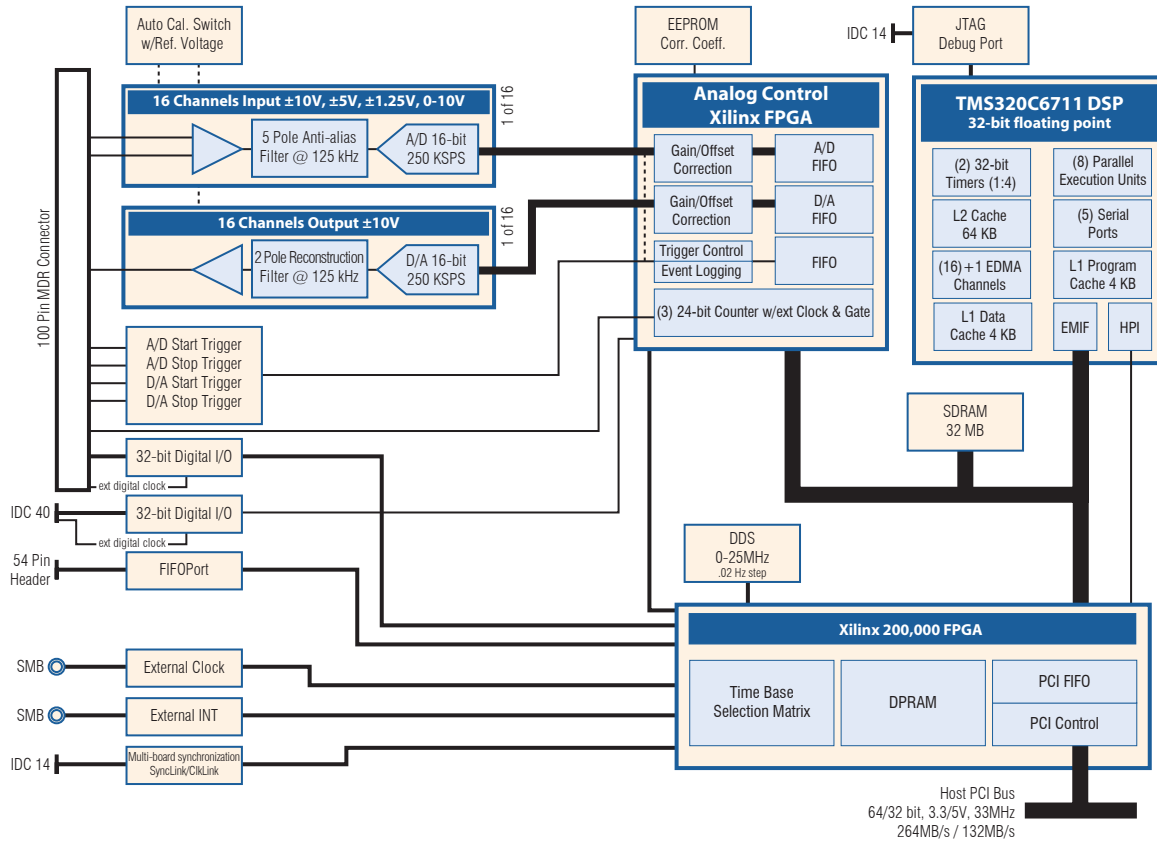
Onboard Peripherals

The Toro features 16 independent channels of 16-bit, 250 kHz A/D and D/A. These are truly independent A/D and D/A channels, which allow simultaneous, non-multiplexed sampling for multiple input/output control systems and applications where channel-to-channel phase matching is important.

Each A/D channel has a high impedance differential input followed by a 5 pole analog anti-alias filter. These A/Ds have low data latency, which is important for servo applications, and are not pipelined like sigma-delta A/Ds. The A/D channels also have digital gain and offset correction in the on-card logic which means no pots to set and reduced analog drift over time. Calibration can be done without disconnecting signal wiring as Toro provides switching to onboard reference voltages. The calibrated A/D samples are buffered into a FIFO of software programmable depth which holds up to 256 samples. With the sample FIFO you won't miss a sample under normal conditions as it alleviates the real-time constraints on the DSP. Input range is software programmable for $\pm 1V$, $\pm 5V$, $\pm 10V$, and 0-10V. Custom ranges are available for OEM applications.

The D/A channels are 16 independent channels of 16-bit, 250 kHz that complement the A/D channels. The D/A channels also have all-digital error correction done in the FPGA and a 256 sample FIFO. Each channel has a 2-pole analog reconstruction filter to smooth the output voltage and deliver a clean signal, free of high frequency artifacts. These D/A converters also have extremely low glitch energy so that sample-to-sample outputs do not have spikes that upset sensitive control systems. Standard output range is $\pm 10V$, and custom ranges are available for OEM applications.

Two high-speed, memory-mapped, 32-bit latches are available to support general-purpose digital I/O. Direction is software-configurable in banks of 8 bits and the port may be software or externally clocked at rates to 10 MHz. The output of an AD9851 digital synthesizer is routed to all 16 analog channels providing a programmable clock spanning 0-25 MHz programmable in increments of .02 Hz. Additionally, the two on-chip timers may be used to trigger conversions.



Time Base, Trigger Modes and Servo-control features

The fields of application for Toro are endless because of the flexible time bases and the wide choice of trigger mechanisms. Toro offers a software configurable time base matrix that allows to drive any time base from a choice of clock sources: on-chip and off-chip timers, DDS, external clock, SyncLink/ClockLink. The selection is simply made with single-line SW commands.

The trigger methods are extremely flexible and accommodate almost any foreseeable synchronization requirements. Toro can quickly be configured for any of the following methods and attributes: External trigger - Analog threshold trigger - Continuous streaming - Framed acquisition (specified by timer or sample counter) - Pre/post trigger sampling - Counted or timed frames - Re-trigger mode. Any trigger register, from timer to analog threshold, can be shared between cards using the SyncLink/ClockLink interface. Please refer to the Matador overview for more details on triggering modes.

Finally, Toro offers two built-in logic features designed specifically for closed-loop control. A decimation mode allows the user to discard A/D readings and deliver data at the desired rate but with minimum latency. The D/As have a delayed trigger mode specific for servo applications. This mode allows the D/As to be updated at a fixed time after A/D conversion occurs. The designer can tune this delay so that the servo calculations are done during this delay, and the D/As are therefore updated as soon as possible. This minimizes data latency and CPU interrupts. Over-run and under-run FIFO registers assist the developer in optimizing settings and monitoring system at run time.

Expansion and Multi-Card Synchronization

Toro's FIFOPort offers high-speed dedicated parallel board-to-board communication between multiple Toro cards and other FIFOPort compatible cards at rates up to 80 MBytes/sec.

Toro provides other features that make system-level integration fast and easy, such as SyncLink/CikLink for multiple card synchronization and Plug-n-Play PCI. The SyncLink/CikLink interface allows up to six unique timing signals and event triggers to be shared between up to 16 cards. Each Toro card has a switch matrix that routes any event trigger to any SyncLink/CikLink port, completely under software control. There is no complex cabling, just a simple connection and software configuration.

Host PC Interface

The Toro card features a 64 bit PCI bus interface capable of busmastering data bursts up to 264 Mbytes/sec. This PCI interface automatically accommodates 64bit/32bit and 3.3V/5V PCI buses running at 33 MHz and configures itself at power-up. The PCI interface built in the firmware manages all busmastering activities independent of the DSP and greatly reduces the complexity of integrating the Toro into host computer applications. Data simply appears in host memory, ready for use by the host program, all at great speed with low latency. Benchmarks of 80MBytes/sec of sustained transfer rates on 32-bit busses have been demonstrated under Win2K. But the most attractive aspect is that these high rates are achieved with no burden at all on the target (i.e. 0% CPU utilization and only 25% bus utilization).

An arbitrated, 256 word dual-port RAM is also provided and is useful for data passing and general communication. This dual-port memory serves a mailbox, or bulletin board, where the DSP and host can swap status and data structures with minimum interference.

Development Tools

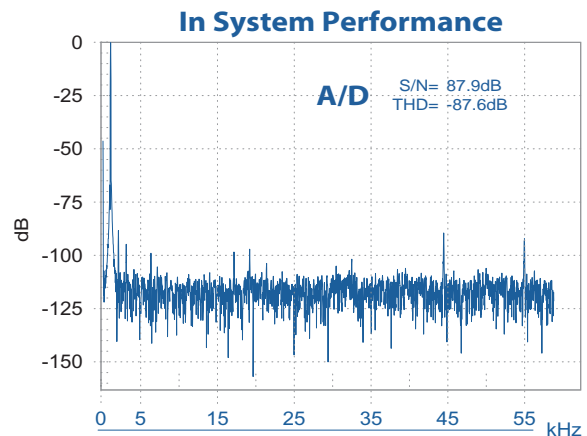
First time buyers of Toro will need to purchase the Toro DevPack. The DevPack includes the Toro card, Code Composer Studio Integrated Development Environment, CodeHammer JTAG Emulator and the Pismo Toolset.

Innovative Integration's Pismo Toolset makes DSP development fast and simple a complete collection of target and host side libraries. The Pismo Toolset includes everything from convenient utility applets allowing download, execution and high level debugging of DSP applications to a complete set of source code examples demonstrating full operation of Toro. The Pismo Toolset is fully supported from within Texas Instruments' Code Composer Studio. Pismo supports and extends each of the features of DSP/BIOS on Toro through a seamless integration of advanced C++ class libraries, BIOS-compliant DSP peripheral device drivers, and clear, illustrative examples. The device drivers fully exploit the available DMA channels in the C6711 chip so that hardware interrupt rate rarely exceeds one kHz! The net effect is that virtually all of the bandwidth of the CPU is available for application processing.

Host side development is accomplished with Armada. This advanced set of tools is integrated into either Borland C++ Builder or Microsoft Visual C++ and offers the most powerful and flexible means to rapidly integrate real time video signal processing into Windows applications. Armada allows development of simple-yet powerful application programs capable of exploiting the full power of Toro including efficient data movement synchronized with the target code, viewing/graphing, signal post-processing or analysis, and disk logging. Host side data streaming and viewing example programs are provided.

OEM Configurations

Toro can be configured to fit your specific requirements and provide an optional mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.



Digital Signal Processor

Texas Instruments TMS320C6711
150MHz
72 Kbytes on-chip program/data memory with efficient L1/L2 cache controller
Two 32-bit timers
16 DMA channels

Memory

32 Mbytes SDRAM (one wait-state)
256 Word dual port RAM with host

Debug Port

JTAG 1149.1 compliant emulation port
Compatible with Code Hammer, XDS-510 or equivalent debugger using TI Code Composer Studio

PCI bus

64/32 bit, 3.3/5V, 33MHz
Interface auto-detects slot type for configuration
Capable of 264 Mbytes/sec data rates on 64 bit busses, 132 Mbytes/sec data rates on 32 bit busses
Busmastering or slave interface
FIFO and dual port memory interfaces
Requires 1MB host memory space

Digital I/O

64 bits programmable as input or output in groups of 8, TTL compatible with 32/-64 mA capability

FIFOPort

64 Mbytes/sec bidirectional data path 256x32 FIFO memory
16-bit data path 32-bit interface to the DSP (requires FIFO cable for proper operation for LVDS signal conditioning)

Timers/Counters

Two on-chip 32-bit timer/counters
80 MHz crystal, external clock, or SyncLink
Three additional 24-bit timers in logic

Analog I/O

A/D

16 independent ch. of 16-bit A/D converters (LTC1606)
250 kHz max. sample rate
5 pole anti-alias filter -3dB @ 125kHz
DC-coupled
Differential Input
All channels clocked from same timebase

A/D Input Range

SW programmable $\pm 1V$, $\pm 10V$, $\pm 5V$, or 0-10V
All-digital offset & gain error correction in FPGA
256 sample FIFO
Onboard reference voltage with converter switches allowing in-system calibration

D/A

16 independent ch. of 16-bit D/A converters (LTC1597)
250 kHz max. sample rate
2 pole reconstruction filter -3 dB @ 125 kHz
All channels clocked from same timebase
Glitch energy: 8nV-s

D/A Output Range

$\pm 10V$ (custom available for OEMs)
All-digital offset & gain error correction in FPGA
256 sample FIFO
Onboard reference voltage with converter switches allowing in-system calibration
Factory Calibrated

Multi-Card Synchronization

Synchronize multiple cards with common trigger or clock
5 TTL compatible signals (master or slave)
One high speed LVDS signal for clocks

Time Bases and Trigger Methods

Conversion Timebase

DDS - 0-25 MHz in 0.02 Hz steps, Two timers, SyncLink/ClockLink, External Clock, Programmable Delay for DAC auto update from A/D conversion for low latency and deterministic control

Start/Stop Triggers

External clock, SyncLink, Software
Programmable timed duration or sample count
Conversion real-time event logging in firmware

Connectors

MDR 100 for analog I/O start/stop triggers, 32-bit digital I/O
14 pin shrouded, polarized male IDC for JTAG
54 pin 2mm header for FIFOPort
40 pin shrouded, polarized male IDC for 32-bit digital I/O
10 pin shrouded, polarized male IDC for SyncLink/ClockLink
SMB for external clock and trigger inputs

Physical card size

Full Size PCI card
Conforms to PCI specification
Max component height: 10mm

Power Requirements

+5V @ 1A; +12V @ 1A

Operating Conditions

10°-55° C

Development Languages

DSP

C or assembler using TI Code Composer studio and Pismo Toolset

PC

MS VC++, Borland C++ Builder

Operating Systems

DSP

DSP/BIOS II

Host PC

Windows2000/XP

Intel processor recommended for max speed in applications using Channelized Mode and Analysis Components, which utilize MMX technology.

Software Selection Guide for Toro

Software Package	Description	Usage/Requirements	Recommendations
Pismo Toolset	Peripheral libraries needed for developing code on this card. Includes host applications and target examples in source form demonstrating use of peripherals on the card, DSP/BIOS peripheral device drivers.	Requires CCStudio* Windows2000/XP compatible.	Required for all first time users. Includes 1 year of technical support.
Caliente DLL	Dynamic link library (DLL) for the Toro.	Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++. Win2000/XP compatible.	Required for interfacing Host side code to DSP. May be used without Armada although not recommended
CCStudio 'C6000	Integrated development environment (IDE) for Target side development/debugging from Texas Instruments.	Requires XDS-510 compatible JTAG emulator for debugging capabilities.	Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator.
Armada	Host side development package using a revolutionary integrated development environment (IDE). Allows user to build/debug sophisticated data acq apps fully using MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) of MFC Classes.	Requires Borland C++ Builder* Microsoft Visual C++.	Included in Pismo Toolset. Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party components.

The Toro Development Package contains all software packages listed above.

*Contact Innovative Integration for current release version.