

TRENDS IN WIRELESS COMMUNICATION BOARDS

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Market demands for higher cellular density in urban areas, broadband internet wireless, and better data security, while using a minimum amount of frequency spectrum is driving wireless developments forward at an amazing speed. Forward leaps in computing power have resulted in GIGAFLOPS (billion floating point operations per seconds) or TERAMACS (trillion multiply-accumulate per second) of processing power that allows telecom engineers to do more and more processing in the digital domain. This offers obvious advantages in flexibility for the implementation of complex algorithms that permit a better utilization of the airwave spectrum, improved transmission quality, and better data security.

SDR

The newest generation of radios are justly called software defined radio (SDR), since the entire signal processing chain, from intermediate frequency (say 50-125MHz) down to baseband frequency (like a voice channel at 8kHz) is done digitally using reconfigurable firmware and software, replacing analog and ASIC digital processing. A typical SDR has these components:

- Analog interface to the RF stage and antenna, via high-speed converters (ADC and DACs) able to digitize a wide portion of the spectrum
- High-speed front-end signal processing including digital down- or up-conversion,
- Protocol-specific processing such as CDMA, TDMA, and satellite communications involve spreading/de-spreading, chip rate and frequency-hop rate recovery- Code/decode functions, including modulation/demodulation, carrier and symbol rate recovery, channel interleaving/de-interleaving
- Data Communications - Interfacing with carrier networks and backbone for data I/O and command-and-control processing, usually handled by general purpose ARM or PowerPC processors and RTOS (Real Time Operating System).

Recent trends in wireless communications boards implement the radio primarily in software through the integration of high performance computing in programmable logic and DSPs with the analog front-end. Designers are able to partition the high speed front-end signal processing from the lower speed baseband and protocol functions for an optimal mix of performance and flexibility.

FPGA's for ultra high-speed processing

The front-end signal processing is usually a very high speed process that is best suited for FPGA processing. The front end signal processing, such as cascaded integrated comb filters and decimators used in up-down-conversion, fit well within most FPGA architectures and are rather simple arithmetic, but intensive in computation cycles because they run at the digitizing rate. These functions are ideal for FPGAs because they scale-up easily for parallel processing and usually do not involve highly complex algorithms. Other functions that require high speed processing in the FPGA typically include spreading/de-spreading, code identification, and error correction. When there is tight integration of the analog and signal processing functions, the designer has complete flexibility for application-specific front-end signal processing for improved signal quality, code identification and carrier acquisition

Programmable logic density and speed are a driving force behind new SDR architectures. FPGA device sizes now approach the 10 million gate mark, offer speeds 200-400 MHz, and allow very complex interfaces to be mapped in logic. There are huge offerings of IP cores that allow firmware engineers to rapidly integrate interfaces such as PCI, Ethernet, T1/E1, RapidIO and HyperTransport as well as communication-specific functions like Digital Down Conversion, FIR and CIC filters, Viterbi and turbo decoder, FFT's, G.709-FEC and POS-PHY interface.

DSP's for smarter, complex processing

The more complex algorithms found in the protocol-specific algorithms are more suited to programmable digital signal processors (DSPs). The number-crunching capability of DSPs, lend themselves perfectly to the baseband processing found in SDR. Algorithms such as demodulation, error correction, data packetizing, and radio control loops are well supported by DSP hardware and software. Many DSPs incorporate hardware acceleration for common functions such as Viterbi decoding, and a large body of software is available for most wireless applications. DSP software development tools now feature high performance RTOS that speed development with standardized plug-in software functions, thereby greatly reducing software development time.

DSP architectures and chip speeds are not only delivering GIGAFLOPS of performance, but also include built-in interfaces like PCI or Utopia (a flexible test and operations PHY interfaces to telephony backbone). Most DSP architectures allow a "glueless" interface between multiple DSPs for efficient clustering of DSPs, and efficient partitioning of the SDR functions. Application specific DSPs are also emerging and offer the optimum set of peripherals for very specific uses like direct audio I/O, video compression or multimedia for PDA's. Finally dual-core devices, combining a traditional DSP architecture with an ARM (or RISC) processor core with shared resources continue to blur the lines between DSP and system-level functions.

Multi-boards for high-channel count and redundancy...

At the system level, SDR systems used for servicing high channel counts and requiring redundancy for high system availability continue to compartmentalize the above processing tasks on separate boards, usually hot-swappable 6U compactPCI. New switched fabric architectures within Compact PCI systems provide an efficient means for high bandwidth, low latency data transfer between boards. Now, high performance serial data buses such as RapidIO or ChannelLink are beginning to replace PCI bus systems, reducing system complexity while delivering data transfer rates 250MBytes/sec and 1+ GByte/sec between boards.

Or integrated architecture for development and maximum bandwidth

Development and test platforms for SDR systems go as far as integrating all the processing stages into a single compactPCI board: analog converters, FPGA and DSP. The advantage of such integrated designs is that it provides radio firmware and software engineers a complete hardware platform that they can be used in the field to develop and test new IP algorithms (intellectual property) or as a powerful, reconfigurable station to test hardware. The advantage here is that all functions of the radio system, excluding network interfaces, can be fully configured and controlled from within a single development environment. There is no need to procure multiple boards and understand the intricacies of efficient synchronization or to learn multiple tool sets.

Wireless board technology continues to be driven by the emergence of newer, more powerful logic and DSP devices, software standards and system architectures. Tighter integration of analog with enormous signal processing power seems to be the name of the game and is leading wireless communications boards to new levels of performance.

