

Innovative Integration

Link44 Hardware Supplement

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The Link44 Hardware Supplement was prepared by the technical staff of Innovative Integration, December 1997

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VSS\4XBUS Modules\LINK44\Documents\Link44.doc

1. Link44 Hardware Functions

The Link44 board provides an interface between Innovative's PC44 and PCI44 cards and hardware compatible with the DSPLink I/O standard.

The module is installed on a host PC44 or PCI44 processor card via the 4XBUS connector, and is interfaced via the user DECODES strobes mapped into the global memory space of the host.

1.1 Installation

The DSPLink connector is installed on the 4XBUS connector on the host card on connector JP54 (on the PC44) or JP10 (on the PCI44). Two standoff locations are also provided to secure the DSPLink44 to the host card.

Please note that the standard Link44 may not be used on PCI44 cards when IndustryPack modules are also in use. Innovative can supply a custom version of the Link44 which has higher connector height for use over IP modules. Contact Innovative for details.

1.2 DSPLink Interface

The Link44 translates accesses by the host processor into the mapped memory space to bus accesses on the DSPLink bus. Host processor address lines 0-7 are connected to the DSPLink connector, providing address sub mapping within the DSPLink address space for multiple devices. The host's data lines 15-31 (i.e. the "high" half of the bus) are connected to the DSPLink data bus pins 0-15, as required by the DSPLink standard. This means that all data transmitted or received to or from the DSPLink bus will be left justified on the host processor's bus.

The Link44 is directly mapped into the host processor card's global memory space using the user decode strobes. Jumper JP2 on the Link44 board allows the module to respond to host bus accesses within any of the four available decode strobe regions. The following table gives the jumper positions for the Link44 memory mappings.

Jumper Position	Function
1-2	USER0
3-4	USER1
5-6	USER2
7-8	USER3

Figure 1: DSPLink Memory Map Jumper Settings

The USERx memory mapping addresses are defined in the host board's Hardware Manual.

DSPLink bus strobes generated by the Link44 are always 3 DSPLink bus clock cycles long, beginning one clock cycle after the beginning of the host bus access to the Link44 module. Please note that the Link44 does not support use of hardware controlled wait states on the DSPLink bus.

DSPLink bus interrupt signals directly drive the external interrupt input 0 and 1 pins on the 4XBUS connector, allowing external hardware to send interrupts to the host processor board. These interrupt signals must be configured on the host card for proper operation. See the host's Hardware Manual for details.

The DSPLink reset line is asserted low in coincidence with the host's hardware reset function. Hardware attached to the Link44 will therefore be held in reset whenever the host board is held in reset.

1.3 DSPLink Connector Pinout

The DSPLink connector allows access to the DSPLink data and control signals.

Connector type: 0.1" double-row shrouded header

Number of pins: 50

Mating connector: AMP 1-111810-0

The following table gives the pin numbers and functions for the DSPLink connector.

Pin Number	Function	Direction (from Link44 host)
2, 11, 24, 33	Digital ground	Power
3-10, 14-16, 19-21	No connect	NA
12	Host H1 clock	O
13	Reset (active low)	O
17	Interrupt 0 (active low)	I
18	Interrupt 1 (active low)	I
22	Enable (active low)	O
23	R/W*	O
25-32	Address 7-0	O
34-49	Data 15-0	I/O

Figure 2: DSPLink Connector Pinout

The following figure gives the pin orientation for the DSPLink connector.

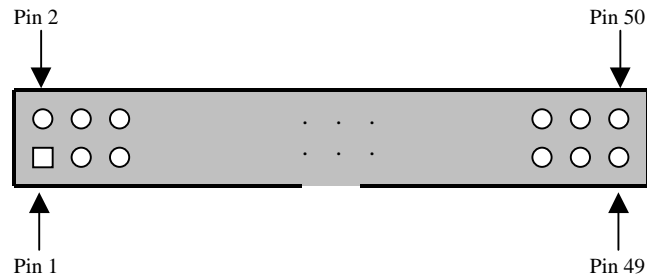


Figure 3: DSPLink Connector Pin Orientation